2Gb DDR3 SDRAM

Lead-Free&Halogen-Free

(RoHS Compliant)

H5TQ2G63BFR

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Revision History

Revision No.	History	Page	Draft Date	Remark
0.1	Preliminary Initial Release		Sep. 2009	Preliminary
0.2	Added Mode Register (MR0, MR1, MR2,MR3, MPR)		Oct. 2009	
0.3	Added IDD value(All Items) @800/9000Mhz Changed AC timing(nRCD, nRC, nRAS, nRP) @800Mhz Changed Speed Bin(CL, CWL & Min/Max timing) @800/900Mhz, 1.0Ghz	65 56 67 ~69	Nov.2009	
0.4	Corrected Typo and wording Changed Single Ended AC and DC Input Levels table Updated AC Overshoot/Undershoot Specification for 1GHz Added timings for 900MHz/1.0GHz(table1) Changed & Updated Idd Specification table Changed Speed Bin for 800/900MHz/1.0Ghz Changed lectrical Characteristics and AC Timing Changed E nged Speed Bin for 800/900MHz	All 34 42 56 65 67~69 71~77 67,68	May. 2010	
0.5	Cha		Aug. 2010	

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1. DESCRIPTION

The H5TQ2G63BFR is a 2,147,483,648-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. Hynix 2Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it.

The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

1.1 Device Features and Ordering Information

1.1.1 FEATURES

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, $\overline{CK}$) operation
- Differential Data Strobe (DQS, $\overline{DQS}$)
- On chip DLL align DQ, DQS and $\overline{DQS}$ transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 6, 8, 9, 10, 11 , 12, 13 7 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0 °C~ 95 °C)
  - 7.8 µs at 0°C ~ 85 °C
  - 3.9 µs at 85°C ~ 95 °C
- Auto Self Refresh supported
- JEDEC standard 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- Write Levelization supported
- On Die Thermal Sensor supported
- 8 bit pre-fetch

1.1.2 ORDERING INFORMATION

Part No.	Power Supply	Clock Frequency	Max Data Rate	Interface	Package
H5TQ2G63BFR-12C	VDD/VDDQ=1.5V	800MHz	1.6Gbps/pin	SSTL-15	96ball FBGA
H5TQ2G63BFR-11C		900MHz	1.8Gbps/pin		
H5TQ2G63BFR-N0C		1.0GHz	2.0Gbps/pin		

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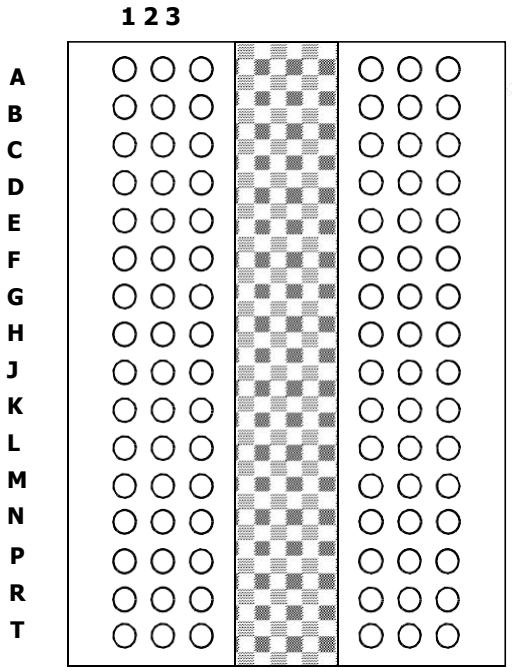
1.2 Package Ball out

1.2.1 x16 Package Ball out

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC		~~WE~~				~~A10/AP~~	~~ZQ~~	NC	L
M	VSS	B	~~BA2~~				~~A15~~	~~VREFCA~~	VSS	M
N	VDD		~~A0~~				~~A12/BC~~	~~BA1~~	VDD	N
P	VSS		~~A2~~				~~A1~~	~~A4~~	VSS	P
R	VDD		~~A9~~				~~A11~~	~~A6~~	VDD	R
T	VSS	R	~~A13~~				~~NC~~	~~A8~~	VSS	T
	1								9	

Note: Green NC balls indicate mechanical support balls with no internal connection



(Top View: See the balls through the Package)

○ Populated ball
+ Ball not populated

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1.3 ROW AND COLUMN ADDRESS TABLE

2Gb

Configuration	128Mb x 16
# of Banks	8
Bank Address	BA0 - BA2
Auto precharge	A10/AP
BL switch on the fly	A12/BC
Row Address	A0 - A13
Column Address	A0 - A9
Page size [1]	2 KB

Note1: Page size is the number of bytes of data delivered from the array to the internal sense amplifiers when an ACTIVE command is registered. Page size is per bank, calculated as follows:

page size = $2^{COLBITS} * ORG / 8$

where COLBITS = the number of column address bits, ORG = the number of I/O (DQ) bits

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1.4 Pin Functional Description

1.4 Pin Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$.
CKE	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, DQS and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU, $\overline{DQSU}$, DQSL, $\overline{DQSL}$, DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/$\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. RESET must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD}, i.e. 1.20V for DC high and 0.30V for DC low.

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, ~~DQL~~, DQS, ~~DQS~~, DQSU, ~~DQSU~~, DQSL, DQSL	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data~~ on DQU0~~-DQU7.~~ The~~ data strobe DQS, DQSL, and DQSU are paired with differential signals DQS, DQSL, and DQSU, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
NC		No Connect: No internal electrical connection is present.
V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage
ZQ	Supply	Reference Pin for ZQ calibration

Note:
Input only pins (BA0-BA2, A0-A15, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, ODT, DM, and $\overline{RESET}$) do not supply termination.

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1.5 Programming the Mode Registers

For application flexibility, various functions, features and modes are programmable in four Mode Registers, provided by the DDR3 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. As the default values of the Mode Registers (MR#) are not defined, contents of Mode Registers must be fully initialized and/or re-initialized, i.e. written, after power-up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents.

The mode register set command cylce time, tMRD is required to complete the write operation to the mode regsiter and is the minimum time required between two MRS commands shown in Figure 4.

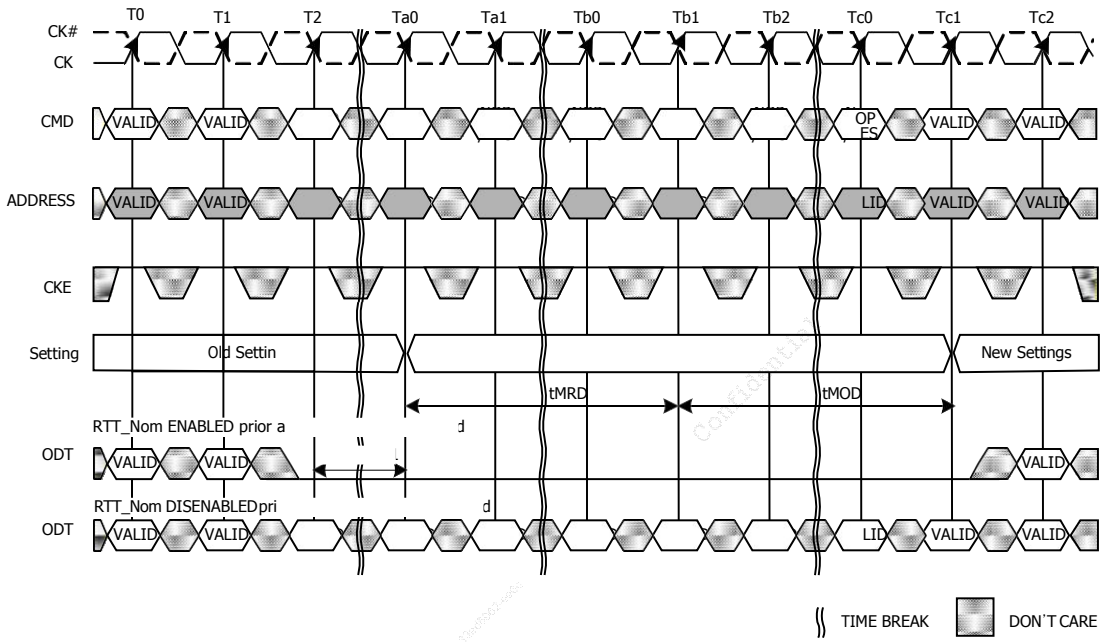


Figure 4. tMRD Timing

The MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, except DLI reset, adn is the minimum time required from an MRS command to a non-MRS command excluding NOP and DES shown in Figure 5.

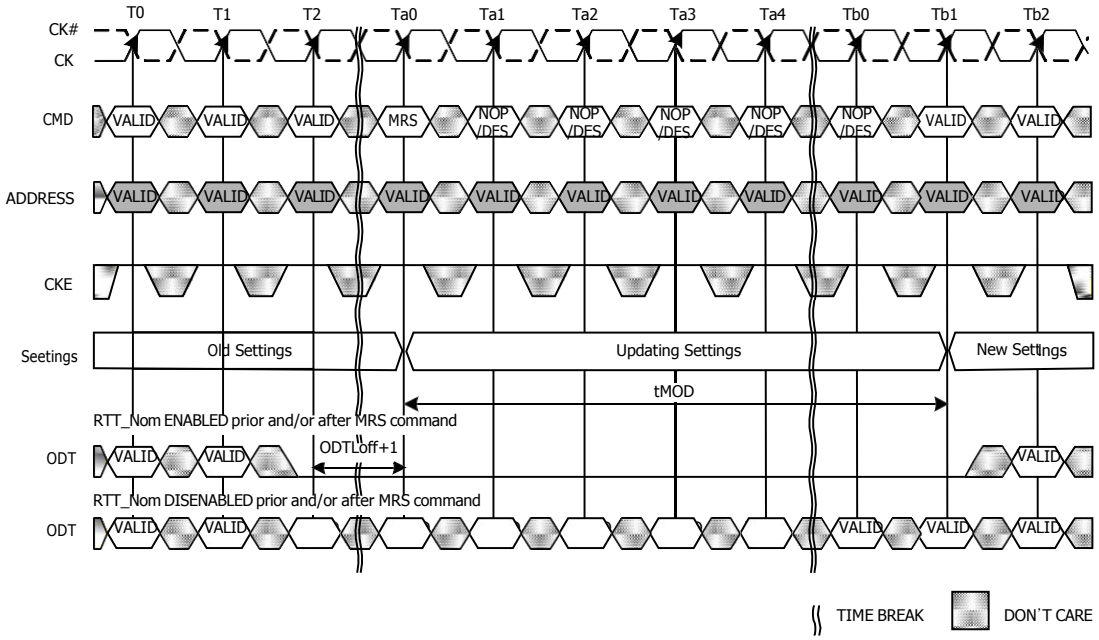
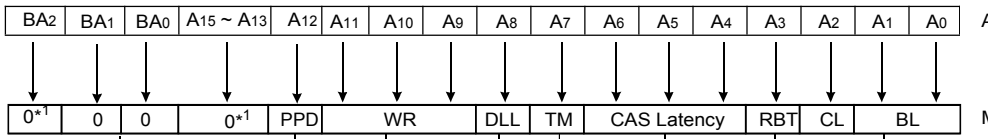


Figure 5. tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM in in idle state, i.e. all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. If the RTT_NOM Feature is enabled in the Mode Register prior and/or after an MRS Commnad, the ODT Signal must comtinuously be registered LOW ensuring RTT is in an off Stated prior to the MRS command. The ODT Signal may be registered high after tMOD has expired. If the RTT_NOM Feature is disabled in the Mode Register prior and after an MRS command, the ODT Signal can be registred either LOW or HIGH before, during and after the MRS command. The mode registers are divided into various fields depending on the functionality and/or modes.

1.6 Mode Register MR0

The mode register stores the data for controlling the various operating modes of DDR3 SDRAM. It controls burst length, read burst type, CAS latency, test mode, DLl reset, WR and DLL control for precharge Power-Down, which include various vendor specific options to make DDR3 SDRAM useful for various applicatons. The mode register is written by asserting low on CS, CAS, WE, BA0, BA1, and BA2, while controlling the states of address pins according to Figure 6.



A8	DLL Reset
0	No
1	Yes

A7	mode
0	Normal
1	Test

A3	Read Burst Type
0	Sequential
1	Interleave

A1	A0	BL
0	1	8 (Fixed)
0	1	BC4 of 8(on the fly)
1	0	BC4 (Fixed)
1	1	Reserved

A12	DLL Control for Precharge PD
0	Slow exit (DLL off)
1	Fast exit (DLL on)

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

Write recovery for autoprecharge

A11	A10	A9	WR(cycles)
0	0	0	16*2
0	0	1	5*2
0	1	0	6*2
0	1	1	7*2
1	0	0	8*2
1	0	1	10*2
1	1	0	12*2
1	1	1	14*2

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11
0	0	0	1	12
0	0	1	1	13
0	1	0	1	14

*1 : BA2 and A13~A15 are RFU and must be programmed to 0 during MRS.
*2: WR(write recovery for autoprecharge) min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
*3: The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency.
*4: The table only shows the encodings for Write Recovery. For actual Write recovery timing, please refer to AC timing table.

Figure 6. DDR3 SDRAM mode register set (MR0)

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1.6.1 Burst Length, Type and Order

Accesses within a given burst may be programmed to suquential or interleaved order. The burst type is selected via bit A3 as shown is Figure 6. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 2. The burst length is defined by bits A0-A1. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC.

Table 2. Burst Type and Burst Order

Burst Length	READ/ WRITE	Starting Column ADDRESS (A2,A1,A0)	burst type = Sequential (decimal) A3 = 0	burst type = Interleaved (decimal) A3 = 1	Notes
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T,	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0,V,V	0,1,2,3,X,X,X,X	0,1,2,3,X,X ,X,X	1,2,4,5
		1,V,V	4,5,6,7,X,X,X,X	4,5,6,7,X,X ,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5 ,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4 ,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7 ,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6 ,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1 ,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0 ,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3 ,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2 ,1,0	2
	WRITE	V,V,V	0,1,2,3,4,5,6,7	0,1,2,3,4,5 ,6,7	2,4

Notes:
1. In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC#, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.
2. 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.
3. T: Ouput driver ofr data and strobes are in high impedance.
4. V: a valid logic level (0 or 1), but respective buffer input ignores level on input pins.
5. X: Don't Care.

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1.6.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 6. CAs Latency is the delay, is clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAm does not support any half clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS latency (CL); RL = AL + CL. For more information on the supported CL and AL settings based on the operating clock frequency, refer to “Standard Speed Bins” . For detailed Read operation refer to “READ Operation”.

1.6.3 Test Mode

The normal operating mode is selected by MR0 (bit A7 = 0) and all other bits set to the desired values shown in Figure 6. Programming bit A7 to a ‘1’ places the DDR3 SDRAM into a test mode that is only used by the DRAM manufacturer and should NOT be used. No operations or functionality is specified if A7 = 1.

1.6.4 DLL Reset

The DLL Reset bit is self-clearing, meaning it returns back to the value of ‘0’ after the DLL reset function has been issued. Once the DLL is enabled, a subsequent DLL Reset should be applied. Any time the DLL reset function is used, tDLLK must be met before any functions that require the DLL can be used (i.e. Read commands or ODT synchronous operations.).

1.6.5 Write Recovery

The Programmed WR value MR0 (bits A9, A10, and A11) is used for the auto precharge feature along with tRP to determine tDAL WR(write recovery for auto-precharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer: WRmin[cycles] = Roundup(tWR[ns]/tCK[ns]). The WR must be programmed to be equal or larger than tWR(min).

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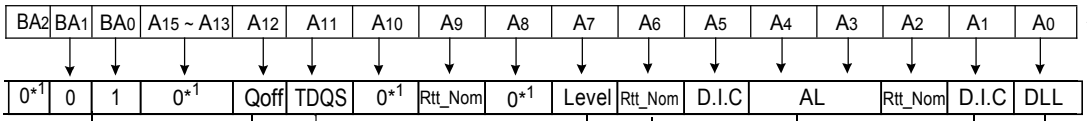
1.6.6 Precharge PD DLL

MR0 (bit A12) is used to select the DLL usage during precharge power-down mode. When MR0 (A12 = 0), or ‘slow-exit’, the DLL is frozen after entering precharge power-down (for potential power savings) and upon exit requires tXPDLL to be met prior to the next valid command. When MR0 (A12 = 1), or ‘fast-exit’, the DLL is maintained after entering precharge power-down requires tXP to be met prior to the next vaild command.

1.7 Mode Register MR1

The Mode Register MR1 stores the data for enabling of disabling the DLL, output driver strength, Rtt_Nom impedance, additive latency, Write leveling enable, TDQS enable and Qoff. The Mode Register 1 is written by asserting low on CS, RAS, CAS, WE, high on BA0 and low on BA1 and BA2, while controlling the states of address pins according to Figure 7.



A11	TDQS enable
0	Disabled
1	Enabled

A9	A6	A2	Rtt_Nom*3
0	0	0	Rtt_Nom disabled
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/12*4
1	0	1	RZQ/8*4
1	1	0	Reserved
1	1	1	Reserved

Note: RZQ = 240Ω

A0	DLL Enable
0	Enable
1	Disable

A7	Write leveling en
0	Disabled
1	Enabled

A4	A3	Additive Late
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

*3: In Write leveling Mode (MR1[bit7]=1) with MR1[bit12]=1, all RTT_Nom settings are allowed; in Write Leveling Mode (MR1[bit7]=1) with MR1[bit12]=0, only RTT_Nom settings of RZQ/2, RZQ4 and RZQ/6 are allowed.

*4: If RTT_Nomm is used during Writes, only the values RZQ/2,RZQ/4 and RZQ/6 are allowed.

A12	Qoff *2
0	Output buffer enabled
1	Output buffer disabled*2

*2: Outputs disabled - DQs, DQSs, DQS#s.

A5	A1	Output Driver Impedence Control
0	0	RZQ/6
0	1	RZQ/7
1	0	RZQ/TBD
1	1	RZQ/TBD

Note: RZQ= 240Ω

BA1	BA0	MR Select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1 : BA2 and A8, A10, and A13~A15 are RFU and must be programmed to 0 during MRS.

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Figure 7. MR1 Definition

1.7.1 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power up initialization, and upon returning to normal operation after having the DLL disabled. During normal operation (DLL-on) with MR1 (A0 = 0), the DLL is automatically disabled when entering Self-Refresh operation and is automatically re-enabled upon exit of Self-Refresh operation. Any time the DLL is enabled and subsequently reset, tDLLK clock cycles must occur before a Read or synchronous ODT command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the tDQSCK, tAON or tAOF parameters. During tDLLK, CKE must continuously be registered high. DDR3 SDRAM does not require DLL for any Write operation, except when RTT_WR is enabled and the DLL is required for proper ODT operation. For more detailed information on DLL Disable operation refer to “DLL-off Mode” on page 37.

The direct ODT feature is not supported during DLL-off mode. The on-die termination resistors must be disabled by continuously registering the ODT pin low and/or by programming the RTT_Nom bits MR1{A9,A6,A2} to {0,0,0} via a mode register set command during DLL-off mode. The dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2 {A10, A9} = {0,0}, to disable Dynamic ODT externally.

1.7.2 Output Driver Impedance Control

The output driver impedance of the DDR3 SDRAM device is selected by MR1 (bits A1 and A5) as shown in Figure 7.

1.7.3 ODT Rtt Values

DDR3 SDRAM is capable of providing two different termination values (Rtt_Nom and Rtt_WR). The nominal termination value Rtt_Nom is programmed in MR1. A seperate value (Rtt_WR) may be programmed in MR2 to enable a unique RTT value when ODT is enabled during writes. The Rtt_WR value can be applied during writes even when Rtt_Nom is disabled.

1.7.4 Additive Latency (AL)

Additive Latency (AL) operation is supported to make command and data bus efficient for sustainable bandwidths in DDR3 SDRAM. In this operation, the DDR3 SDRAM allows a read or write command (either with or without auto-precharge) to be issued immediately after the active command. The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings. Write Latency (WL) is controlled by the sum of the AL and CAS Write Latency (CWL) register settings. A summary of the AL register options are shown in Table.

Table 3. Additive Latency (AL) Settings

A4	A3	AL
0	1	0 (AL Disabled)
0	1	CL - 1
1	0	CL - 2
1	1	Reserved

Note: AL has a value of CL - 1 or CL - 2 as per the CL values programmed in the MR0 register

1.7.5 Write leveling

For better signal integrity, DDR3 memory module adopted fly-by topology for the commands, addresses, control signals and clocks. The fly-by topology has benefits from reducing number of stubs and their length but in other aspect, caused flight time skew between clock and strobe at every DRAM on DIMM. It makes it difficult for the Controller to maintain tDQSS, tDSS and tDSH specification. Therefore, the DDR3 SDRAM supports a ‘write leveling’ feature to allow the controller to compensate for skew. See “Write Leveling” for mode details.

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1.7.6 Output Disable

The DDR3 SDRAM oupputs may be enabled/disabled by MR1 (bit A12) as shown in Figure 7. When this feature is enabled (A12=1), all output pins (DQs, DQS, DQS, etc.) are disconnected from the device removing any loading of the output drivers. This feature may be useful when measuring module power for example. For normal operation, A12 should be set to '0'.

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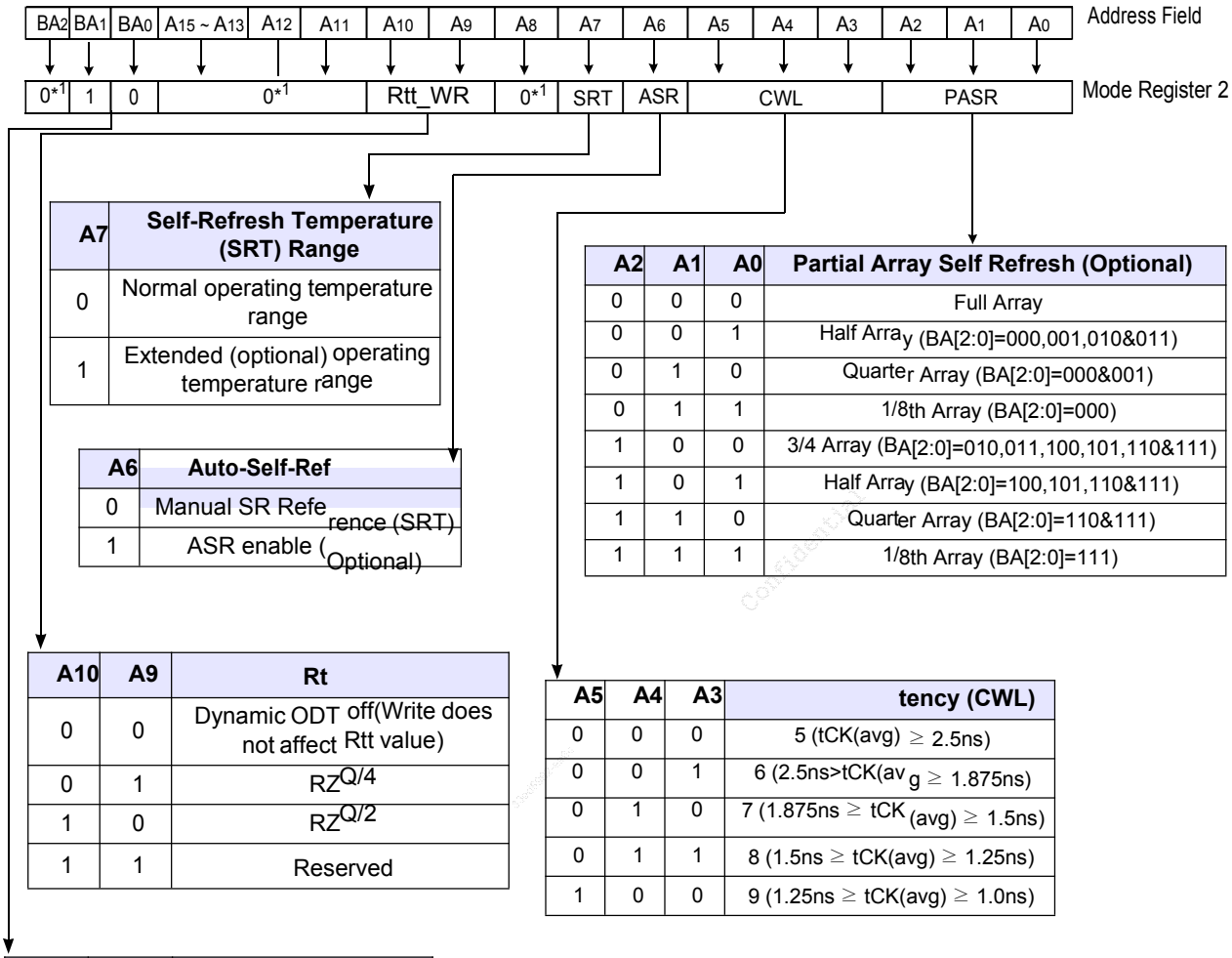
1.8 Mode Register MR2

The Mode Register MR2 stores the data for controlling refresh related features, Rtt_WR impedance, and CAS wire latency.The Mode Register 2 is written by asserting low on CS, RAS, CAS, We, high on BA1 and low on BA0 and BA2, while controlling the states of address pins according to the table below.

MR2 Programming:



A7	Self-Refresh Temperature (SRT) Range
0	Normal operating temperature range
1	Extended (optional) operating temperature range

A6	Auto-Self-Ref
0	Manual SR Reference (SRT)
1	ASR enable (Optional)

A2	A1	A0	Partial Array Self Refresh (Optional)
0	0	0	Full Array
0	0	1	Half Array (BA[2:0]=000,001,010&011)
0	1	0	Quarter Array (BA[2:0]=000&001)
0	1	1	1/8th Array (BA[2:0]=000)
1	0	0	3/4 Array (BA[2:0]=010,011,100,101,110&111)
1	0	1	Half Array (BA[2:0]=100,101,110&111)
1	1	0	Quarter Array (BA[2:0]=110&111)
1	1	1	1/8th Array (BA[2:0]=111)

A10	A9	Rtt
0	0	Dynamic ODT off(Write does not affect Rtt value)
0	1	RZQ/4
1	0	RZQ/2
1	1	Reserved

A5	A4	A3	tency (CWL)
0	0	0	5 (tCK(avg) ≥ 2.5ns)
0	0	1	6 (2.5ns>tCK(avg ≥ 1.875ns)
0	1	0	7 (1.875ns ≥ tCK (avg) ≥ 1.5ns)
0	1	1	8 (1.5ns ≥ tCK(avg) ≥ 1.25ns)
1	0	0	9 (1.25ns ≥ tCK(avg) ≥ 1.0ns)

BA1	BA0	MR mode
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

*1 : BA2, A5, A8, A11~A15 are RFU and must be programmed to 0 during MRS.
*2 : The Rtt_WR value can be applied during wirtes even when Rtt_Nom is disabled. During write leveling, Dynamic ODT is not available.

Figure 8. MR2 Definition

1.8.1 Partial Array Self-Refresh (PASR)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to detemine if DDR3 SDRAM devices support the following options or requirements referred to in this material. If PASR (Partial Array Self-Refresh) is enabled, data located in areas of the array beyond the specified address range shown in Figure 8 wil be maintains if tREFI conditions are met and no Self-Refresh command is issued.

1.8.2 CAS Write Latency (CWL)

The CAS Write Latency is defined by MR2 (bits A3-A5), as shown in Figure 8. CAS Write Latency is the delay, in clock cycles, between the internal Write command and the availability of the first bit of input data. DDR3 SDRAM does not support any half clock latencies. The overall Write Latency (WL) is defined as Additive Latency (AL) + CAS Write Latency (CWL); WL = AL + CWL. For detailed Write operation refer to “WRITE Operation”.

1.8.3 Auto Self-Refresh (ASR) and Self-Refresh Temperature (SRT)

Optional in DDR3 SDRAM: Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determaine if DDR3 SDRAM devices support the following options or requirements referred to in this material. DDR3 SDRAM’s must support Self-Refresh operation at all supported temperatures. Applications requiring Self-Refresh operation in the Extended Temperature Range must use the optional ASR function or program the SRT bit appropriately.

1.8.4 Dynamic ODT (Rtt_WR)

DDR3 SDRAM introduces a new feature “Dynamic ODT”. In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR3 SDRAM can be changed without issuing an MRS command. MR2 Register locations A9 and A10 configure the Dynamic ODT setings. In Write leveling mode, only RTT_Nom is available. For details on Dynamic ODT operation, refer to “Dynamic ODT”.

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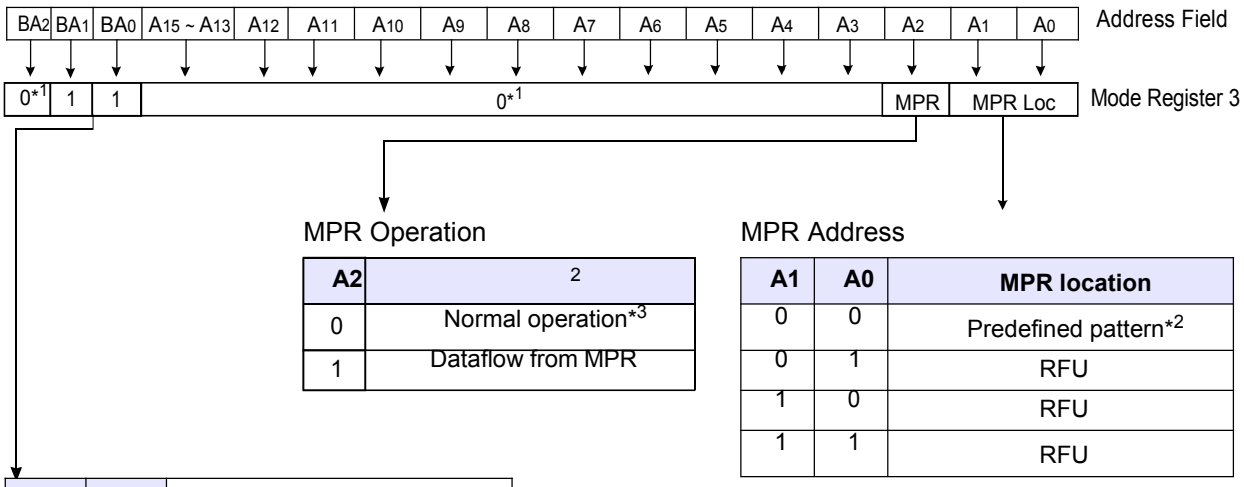
1.9 Mode Register MR3

The Mode Register MR3 controls Multi purpose registers. The Mode Register 3 is written by asserting low on CS, RAS, CAS, WE, high on BA1 and BA0, and low on BA2 while controlling the states of address pins according to the table below.

MR3 Programming:



MPR Operation

A2	2
0	Normal operation*3
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern*2
0	1	RFU
1	0	RFU
1	1	RFU

BA1	BA0	MR S
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

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*1 : BA2, A3-A15 are RFU and must be programmed to 0 during MRS.
*2 : The predefined pattern will be used for read synchronization.
*3 : When MPr control is set for normal operation (MR3 A[2]=0) then MR3 A[1:0] will be ignored.

Figure 9. MR3 Definition

1.10 Multi-Purpose Register (MPR)

The Multi Purpose Register(MPR) function is used to Read out a predefined system timing calibration bit sequence. To enable the MPR, a MODE Register Set(MRS) command must be issued to MR3 Register with bit A2=1. Prior to issuing the MRS command, all banks must be in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. When the MPR is enabled, only RD ro RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled(MR3 bit A2=0). Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode. For detailed MPR operation refer to “Multi Purpose Register”.

1.10.1 Multi Purpose Register

The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence. The basic concept of the MPR is shown in Figure 10.

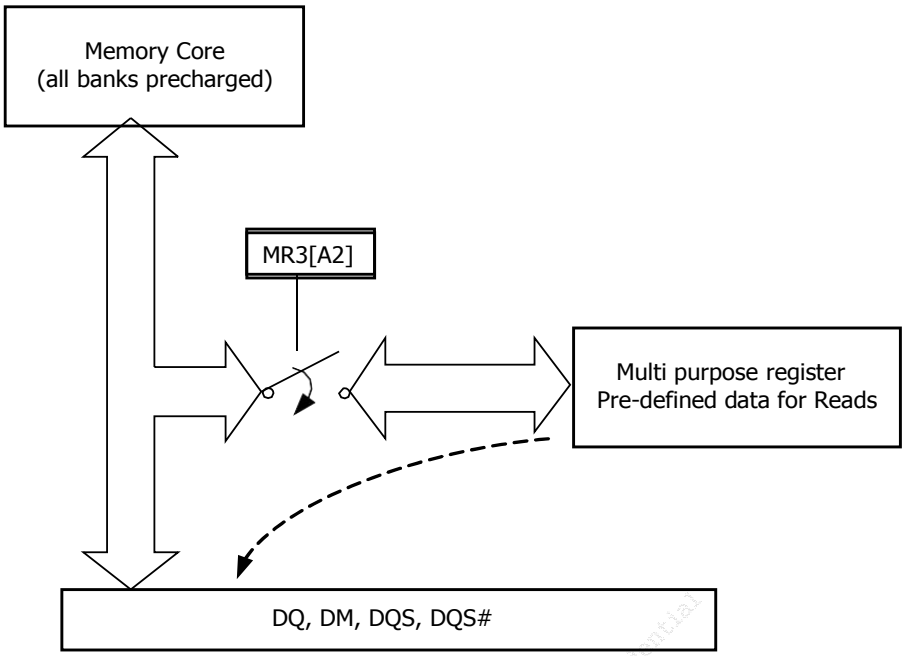

Figure 10. MPR Block Diagram

The enable the MPR, a MODE Register Set (MRS) command must be issued to MR3 Register with bit A2=1, as shown in Table 5. Prior to issuing the MRS command, all banks must be in the idle in the idle state (all banks precharged and tRP met). Once the MPR is enabled, any subsequent RD or RDA commands will be redirected to the Multi Purpose Register. The resulting operation when a RD or RDA command is issued is defined by MR3 bits A[1:0] when the MPR is enabled as shown in Table 6. When the MPR is enabled, only RD or RDA commands are allowed until a subsequent MRS command is issued with the MPR disabled(MR3 bit A2=0). Note that in MPR mode RDA has the same functionality as a READ command which means the auto precharge part of RDA is ignored. Power-Down mode, Self-Refresh, and any other non-RD/RDA command is not allowed during MPR enable mode. The RESET function is supported during MPR enable mode.

Table 5. MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function
MPR	MPR-Loc	
0b	don't care (0b or 1b)	Normal operation, no MPR transaction. All subsequent Reads will come from DRAM array. All subsequent Write will go to DRAM array.
1b	See Table 12	Enable MPR mode, subsequent RD/RDA commands defined by MR3 A[1:0]

1.10.2 MPR Functional Description

- One bit wide logical interface via all DQ pins during READ operation.
- Register Read on x16:
  - DQL[7:1] and DQU[7:1] either drive the same information as DQ[0], or they drive 0b.
- Addressing during for Multi Purpose Register reads for all MPR agents:
  - BA[2:0]: don't care
  - A[1:0]: A[1:0] must be equal to '00'b.Data read burst order in nibble is fixed.
  - A[2]: For BL=8, A[2] must be equal to 0b, burst order is fixed to [0,1,2,3,4,5,6,7],* For Burst Chop 4 cases, the burst order is switched on nibble base A[2]=0b, Burst order: 0,1,2,3* A[2]=1b, Burst order: 4,5,6,7*
  - A[9:3]: don't care
  - A10/AP: don't care
  - A12/BC: Selects burst chop mode on-the-fly, if enabled within MR0.
  - A11,A13,...(if available): don't care
- Regular interface functionality during register reads:
  - Support two Burst Ordering which are switched with A2 and A[1:0]=00b.
  - Support of read burst chop (MRS and on-the-fly via A12/BC)
  - All other address bits (remaining column address bits including A10, all bank address bits) will be ignored by the DDR3 SDRAM.
  - Regular read latencies and AC timings apply.
  - DLL must be locked prior to MPR Reads.

Note: * Burst order bit 0 is assigned to LSB and burst order bit 7 is assigned to MSB of the selected MPR agent.

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1.10.3 MPR Register Address Definition

Table 6 provides an overview of the available data locations, how they are addressed by MR3 A[1:0] during a MRS to MR3, and how their individual bits are mapped into the burst order bits during a Multi Purpose Register Read.

Table 6. MPR MR3 Register Definition

MR3 A[2]	MR3 A[1:0]	Function	Burst Length	Read Address A[2:0]	Burst Order and Data Pattern
1b	00b	Read predefined Pattern for System Calibration	BL8	000b	Burst order 0,1,2,3,4,5,6,7 Pre-defined Data Pattern [0,1,0,1,0,1,0,1]
			BC4	000b	Burst order 0,1,2,3 Pre-defined Data Pattern [0,1,0,1]
			BC4	100b	Burst order 4,5,6,7 Pre-defined Data Pattern [0,1,0,1]
1b	01b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	10b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
1b	11b	RFU	BL8	000b	Burst order 0,1,2,3,4,5,6,7
			BC4	000b	Burst order 0,1,2,3
			BC4	100b	Burst order 4,5,6,7
Note: Burst order bit 0 is assigned to LSB and the burst order bit 7 is assigned to MSB of the selected MPR agent.					

1.10.4 Relevant Timing Parameters

The following AC timing parameters are important for operating the Multi Purpose Register: tRP, tMRD, tMOD, and tMPRR. For more details refer to “Electrical Characteristics & AC Timing for 800Mhz” on page 71.

1.10.5 Protocol Example

Protocol Example (This is one example):

Read out predetermined read-calibration pattern.

Description: Multiple reads from Multi Purpose Register, in order to do system level read timing calibration based on predetermined and standardized pattern.

Protocol Steps:

- Precharge All.
- Wait until tRP is satisfied.
- MRS MR3, Opcode “A2=1b” and “A[1:0]=00b”
  - Redirect all subsequent reads into the Multi Purpose Register, and load Pre-defined pattern into MPR.
- Wait until tMRD and tMOD are satisfied (Multi Purpose Register is then ready to be read). During the

- period MR3 A2=1, no data write operation is allowed.
- Read:
  - A[1:0]='00'b (Data burst order is fixed starting at nibble, always 00b here)
  - A[2]='0'b (For BL=8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12/BC=1 (use regular burst length of 8)
  - All other address pins (including BA[2:0] and A10/AP): don't care
- After RL=AL+CL, DRAM bursts out the predefined Read Calibration Pattern.
- Memory controller repeats these calibration reads until read data capture at memory controller is optimized.
- After end of last MPR read burst, wait until tMPRR is satisfied.
- MRS MR3, Opcode "A2=0b" and "A[1:0]=valid data but value are don't care"
  - All subsequent read and write accesses will be regular reads and writes from/to the DRAM array.
- Wait until tMRD and tMOD are satisfied.
- Continue with "regular" DRAm commands, like activate a memory bank for regular read or write access,...
-
-

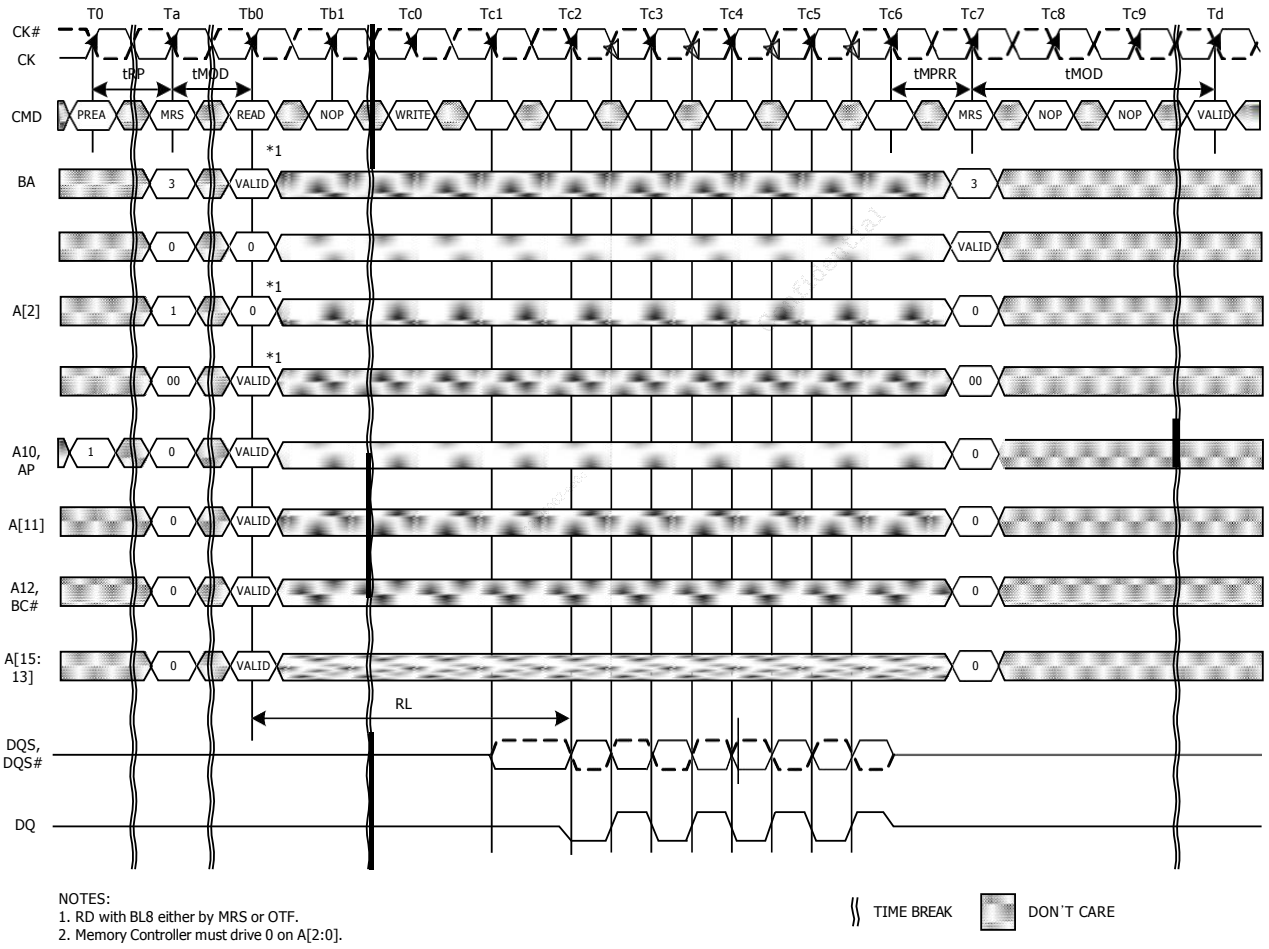


Figure 11. MPR Readout of predefined pattern, BL8 fixed burst order, single readout

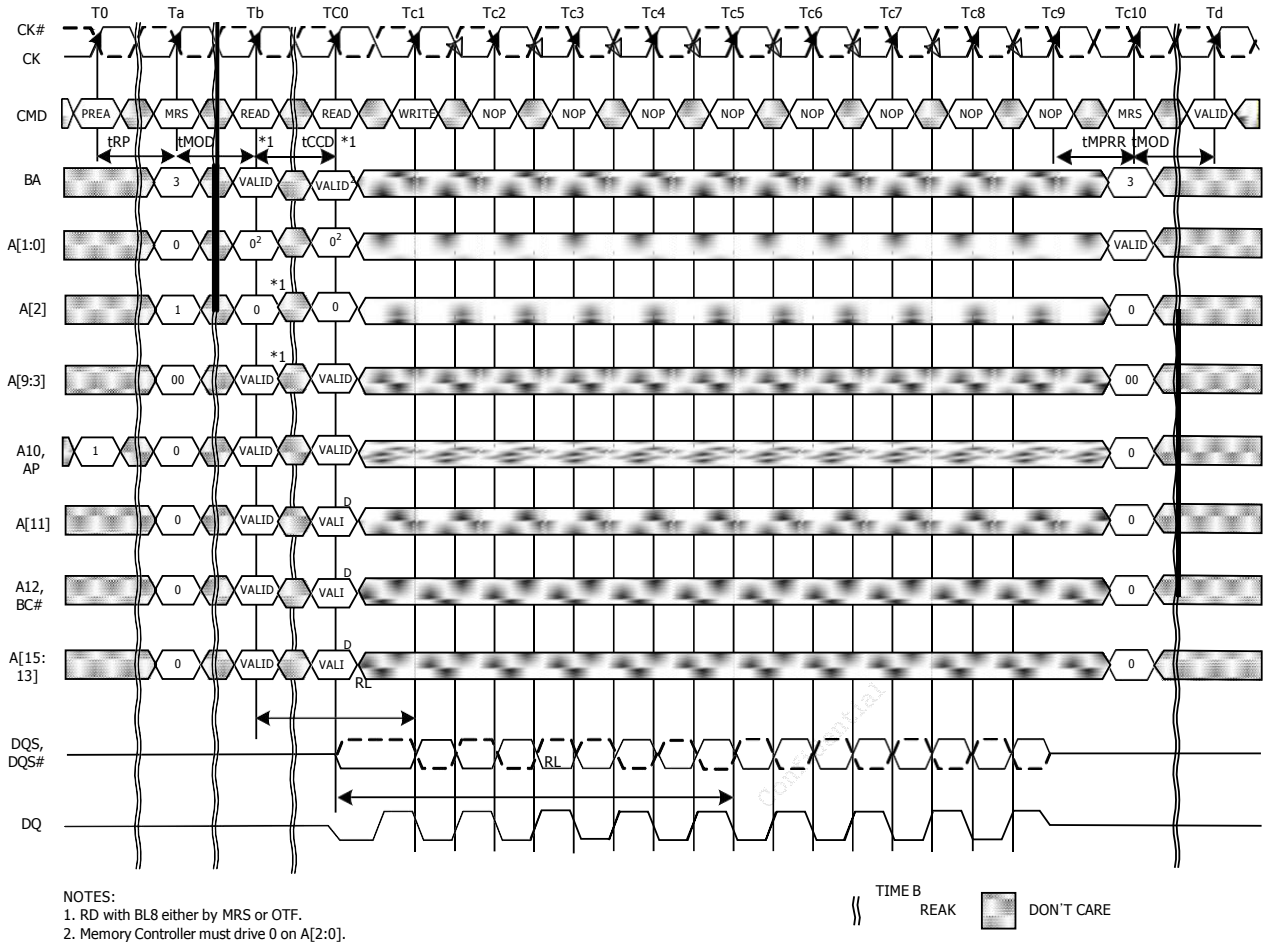
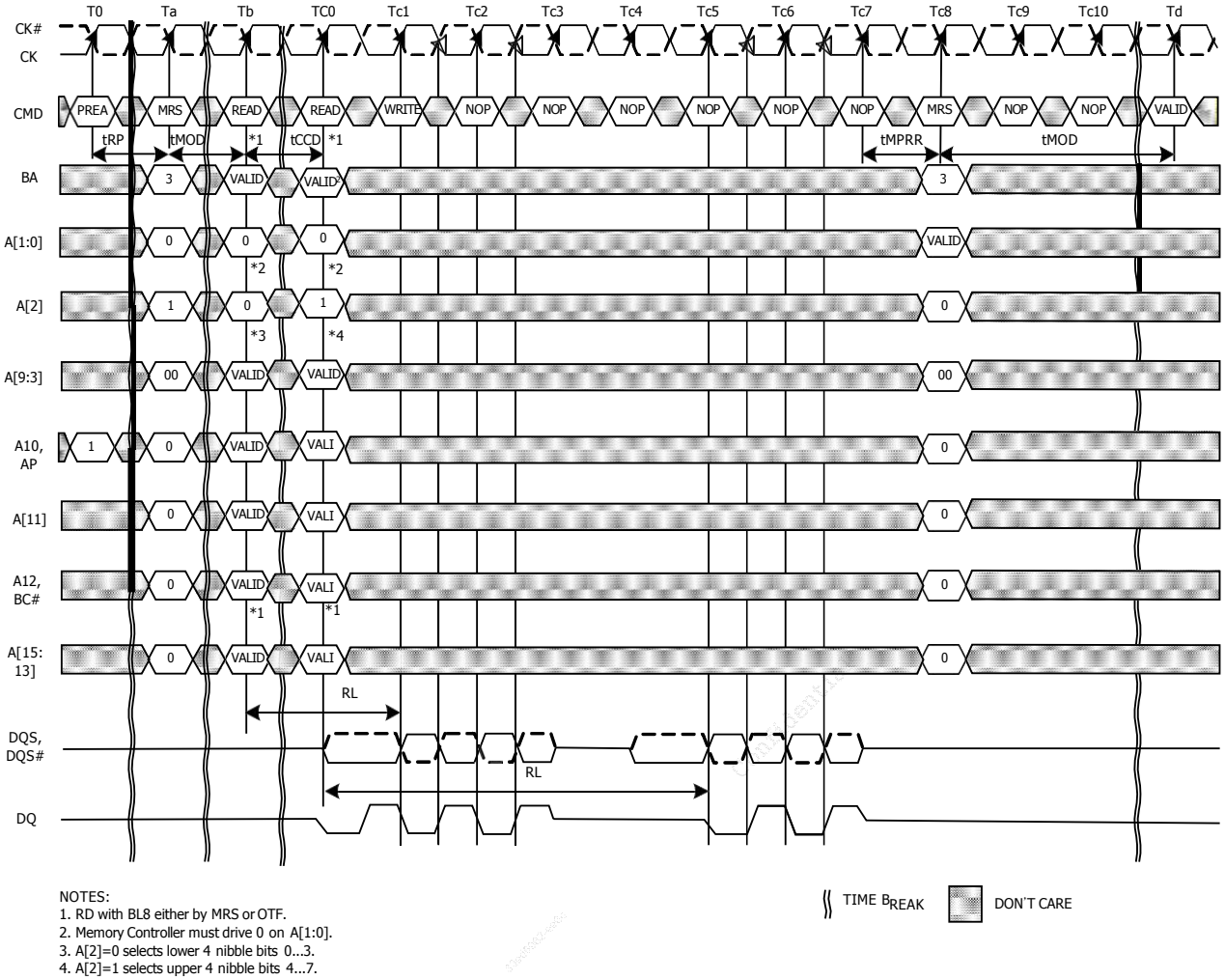
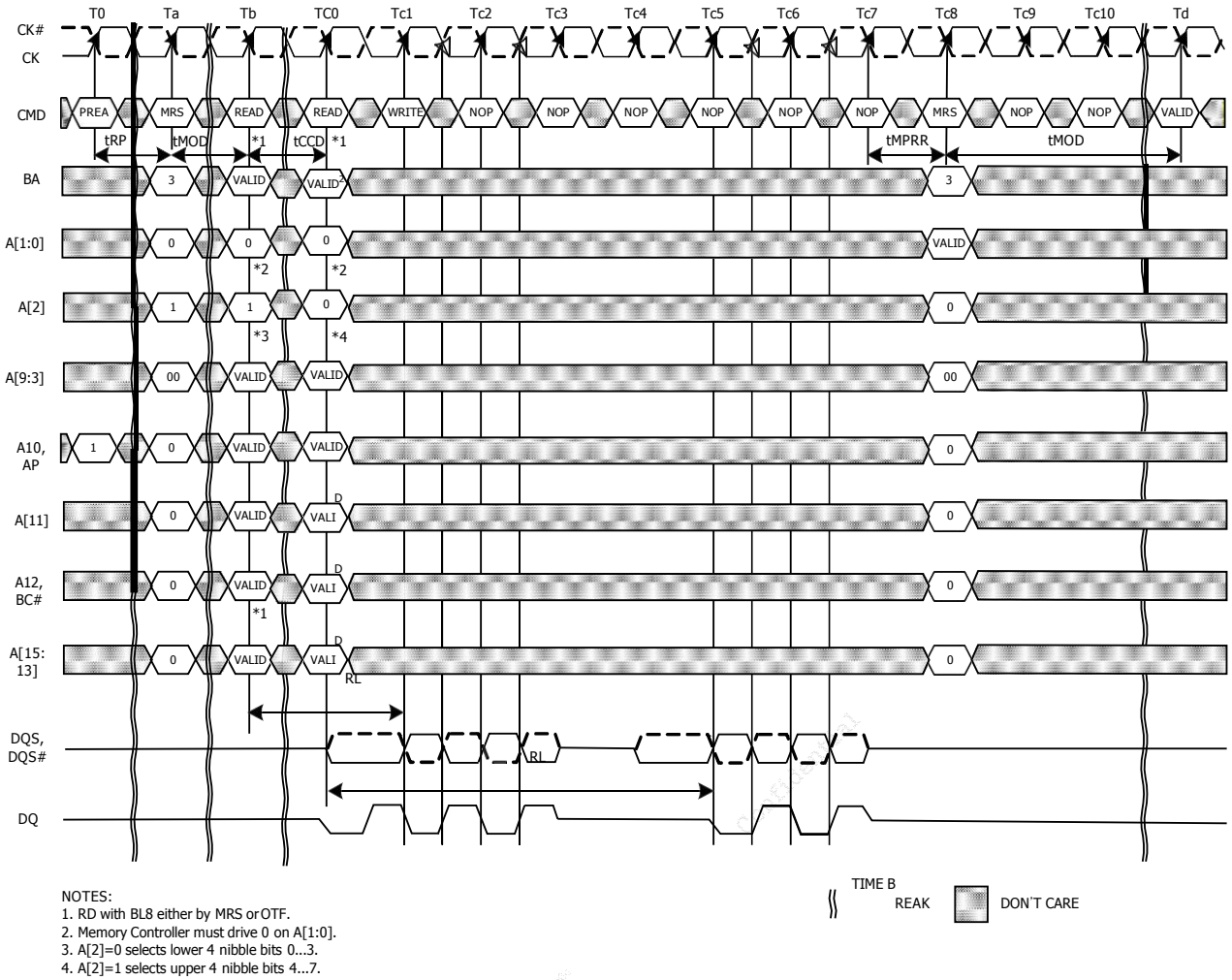


Figure 12. MPR Readout of predefined pattern, BL8 fixed burst order, back-to-back readout



NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0...3.
4. A[2]=1 selects upper 4 nibble bits 4...7.

Figure 13. MPR Readout of predefined pattern, BC4, lower nibble then upper readout



NOTES:
1. RD with BL8 either by MRS or OTF.
2. Memory Controller must drive 0 on A[1:0].
3. A[2]=0 selects lower 4 nibble bits 0...3.
4. A[2]=1 selects upper 4 nibble bits 4...7.

Figure 14. MPR Readout of predefined pattern, BC4, upper nibble then lower readout

2. Command Description

2.1 Command Truth Table

(a) note 1,2,3,4 apply to the entire Command Truth Table

(b) Note 5 applies to all Read/Write command

[BA = Bank Address, RA = Rank Address, CA = Column Address, $\overline{BC}$ = Burst Chop, X = Don't Care, V = Valid]

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA3	A13-A15	A12-$\overline{BC}$	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Refresh	REF	H	H	L	L	L	H	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	L	L	H	V	V	V	V	V	7,9,12
Self Refresh Exit	SRX	L	H	H	V	V	V	V	V	V	V	V	7,8,9,12
		H	H	L	H	H	H	BA					
Single Bank Precharge	PRE	H	H	L	L	H	L	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	L	H	H	BA	V	V	H	V	
Bank Activate	ACT	H	H	L	H	L	L	BA	RFU	Row Address (RA)			
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Write (BC4, on the Fly)	WRS4	H H L H L L BA RFU								L	L	CA	
Write (BL8, on the Fly)	WRS8									H	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	L	L	BA	RFU	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	L	L	BA	RFU	L	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	L	L	BA	RFU	H	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	L	H	BA	RFU	L	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	L	H	BA	RFU	H	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	L	H	BA	RFU	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	L	H	BA	RFU	L	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	L	H	BA	RFU	H	H	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11
Power Down Entry	PDE	H	L	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						

Function	Abbreviation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA0-BA3	A13-A15	A12-$\overline{BC}$	A10-AP	A0-A9, A11	Notes
		Previous Cycle	Current Cycle										
Power Down Exit	PDX	L	H	L	H	H	H	V	V	V	V	V	6,12
				H	V	V	V						
ZQ Calibration Long	ZQCL	H	H	L	H	H	L	X	X	X	H	X	
ZQ Calibration Short	ZQCS	H	H	L	H	H	L	X	X	X	L	X	

Notes:

1. All DDR3 SDRAM commands are defined by states of $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.
2. $\overline{RESET}$ is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
3. Bank addresses (BA) determine which bank is to be operated upon. For (E)MRS BA selects an (Extended) Mode Register.
4. "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
5. Burst reads or writes cannot be terminated or interrupted and Fixed/on the Fly BL will be defined by MRS.
6. The Power Down Mode does not perform any refresh operation.
7. The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
8. Self Refresh Exit is asynchronous.
9. VREF (Both VrefDQ and VrefCA) must be maintained during Self Refresh operation.
10. The No Operation command should be used in cases when the DDR3 SDRAM is in an idle or wait state. The purpose of the No Operation command(NOP) is to prevent the DDR3 SDRAM from registering any unwanted commands between operations. A No Operation command will not terminate a previous operation that is still executing, such as a burst read or write cycle.
11. The Deselect command performs the same function as No Operation command.
12. Refer to the CKE Truth Table for more detail with CKE transition.

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2.2 CKE Truth Table

a) Notes 1-7 apply to the entire CKE Truth Table.
b) CKE low is allowed only if tMRD and tMOD are satisfied.

Current State[2]	CKE		Command (N)[3] RAS, CAS, WE, CS	Action (N)[3]	Notes
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power-Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT or NOP	Power-Down Exit	11,14
Self-Refresh	L	L	X	Maintain Self-Refresh	15,16
	L	H	DESELECT or NOP	Self-Refresh Exit	8,12,16
Bank(s) Active	H	L	DESELECT or NOP	Active Power-Down Entry	11,13,14
Reading	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Writing	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Precharging	H	L	DESELECT or NOP	Power-Down Entry	11,13,14,17
Refreshing	H	L	DESELECT or NOP	Precharge Power-Down Entry	11
All Banks Idle	H	L	DESELECT or NOP	Precharge Power-Down Entry	11,13,14,18
	H	L	REFRESH	Self-Refresh	9,13,18
For more details with all signals See “2.1 Command Truth Table” on page 29 ..					10

Notes:

1. CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.
2. Current state is defined as the state of the DDR3 SDRAM immediately prior to clock edge N.
3. COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N), ODT is not included here.
4. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
5. The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.
6. tCKEmin of [TBD] clocks means CKE must be registered on [TBD] consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the [TBD] clocks of registration. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of tIS + [TBD] + tIH.
7. DESELECT and NOP are defined in the Command Truth Table.
8. On Self-Refresh Exit DESELECT or NOP commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.
9. Self-Refresh mode can only be entered from the All Banks Idle state.
10. Must be a legal command as defined in the Command Truth Table.
11. Valid commands for Power-Down Entry and Exit are NOP and DESELECT only.
12. Valid commands for Self-Refresh Exit are NOP and DESELECT only.
13. Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions **see 8.1 on page 41**.
14. The Power-Down does not perform any refresh operations.
15. “X” means “don’t care” (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.
16. VREF (Both Vref_DQ and Vref_CA) must be maintained during Self-Refresh operation.
17. If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.
18. ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP, tXPDLL, etc).

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3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VDDQ	Voltage on VDDQ pin relative to Vss	- 0.4 V ~ 1.975 V	V	,3
VIN, VOUT	Voltage on any pin relative to Vss	- 0.4 V ~ 1.975 V	V	
TSTG	Storage Temperature	-55 to +100		, 2

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must not be greater than 0.6XVDDQ,When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

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4. Operating Conditions

4.1 OPERATING TEMPERATURE CONDITION

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating Temperature (Tcase)	0 to 85	°C	2
	Extended Temperature Range	85 to 95	°C	1,3

Notes:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 - 85oC under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. (This double refresh requirement may not apply for some devices.) It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b).

4.2 RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Notes:

1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

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5. AC and DC Input Measurement Levels

5.1 AC and DC Logic Input Levels for Single-Ended Signals

Single Ended AC and DC Input Levels

Symbol	Parameter	Min	Max	Unit	Notes
VIH(DC)	DC input logic high	Vref + 0.100	VDD	V	1
VIL(DC)	DC input logic low	VSS	Vref - 0.100	V	1
VIH(AC)	AC input logic high	Vref + 0.175	-	V	1, 2
VIL(AC)	AC input logic low		Vref - 0.175	V	1, 2
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	V	3, 4
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Notes:

1. For DQ and DM, Vref = VrefDQ. For input any pins except $\overline{\text{RESET}}$, Vref = VrefCA.
2. The "t.b.d." entries might change based on overshoot and undershoot specification.
3. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from $V_{Ref(DC)}$ by more than +/-1% VDD (for reference: approx. +/- 15 mV).
4. For reference: approx. VDD/2 +/- 15 mV.

The dc-tolerance limits and ac-noise limits for the reference voltages VRefCA and VRefDQ are illustrated in below Figure. It shows a valid reference voltage VRef (t) as a function of time. (VRef stands for VRefCA and VRefDQ likewise).
VRef (DC) is the linear average of VRef (t) over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements in Table.
Furthermore VRef (t) may temporarily deviate from VRef (DC) by no more than +/- 1% VDD.

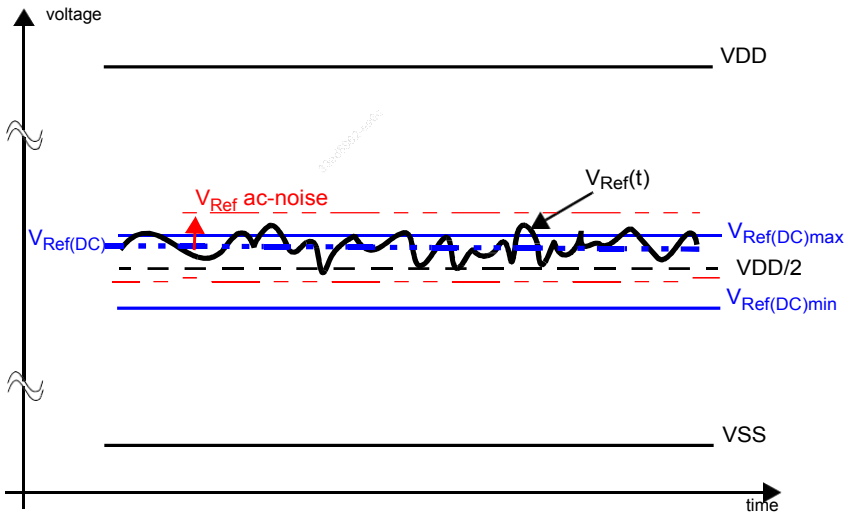


Illustration of Vref (DC) tolerance and Vref ac-noise limits

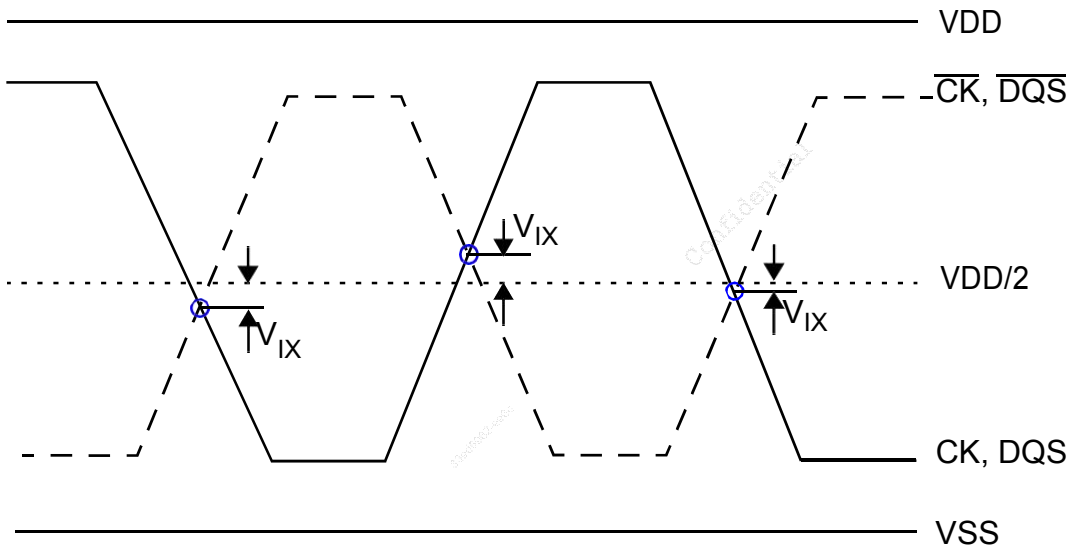
5.2 AC and DC Logic Input Levels for Differential Signals

Symbol	Parameter	Min	Max	Unit	Notes
VIHdiff	Differential input logic high	+ 0.200	-	V	1
VILdiff	Differential input logic low		- 0.200	V	1

Note1.
Refer to “Overshoot and Undershoot Specification on page 25”

5.3 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, CK and DQS, DQS) must meet the requirements below table. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signal to the midlevel between of VDD and VSS.



Vix Definition

Cross point voltage for differential input signals (CK, DQS)

Symbol	Parameter	Min	Max	Unit	Notes
V_{IX}	Differential Input Cross Point Voltage relative to VDD/2	- 150	150	mV	

5.4 Slew Rate Definitions for Single Ended Input Signals

5.4.1 Input Slew Rate for Input Setup Time (tIS) and Data Setup Time (tDS)

Setup (tIS and tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIH (AC) min. Setup (tIS and tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VRef and the first crossing of VIL (AC) max.

5.4.2 Input Slew Rate for Input Hold Time (tIH) and Data Hold Time (tDH)

Hold nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL (DC) max and the first crossing of VRef. Hold (tIH and tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH (DC) min and the first crossing of VRef.

Single-Ended Input Slew Rate Definition

Description	Measured		Defined by	Applicable for
	Min	Max		
Input slew rate for rising edge	Vref	VIH (AC) min	$\frac{\text{VIH (AC) min - Vref}}{\text{Delta TRS}}$	Setup (tIS, tDS)
Input slew rate for falling edge	Vref	VIL (AC) max	$\frac{\text{Vref - VIL (AC) max}}{\text{Delta TFS}}$	
Input slew rate for rising edge	VIL (DC) max	Vref	$\frac{\text{Vref - VIL (DC) max}}{\text{Delta TFH}}$	Hold (tIH, tDH)
Input slew rate for falling edge	VIH (DC) min	Vref	$\frac{\text{VIH (DC) min - Vref}}{\text{Delta TRH}}$	

Input Nominal Slew Rate Definition for Single-Ended Signals

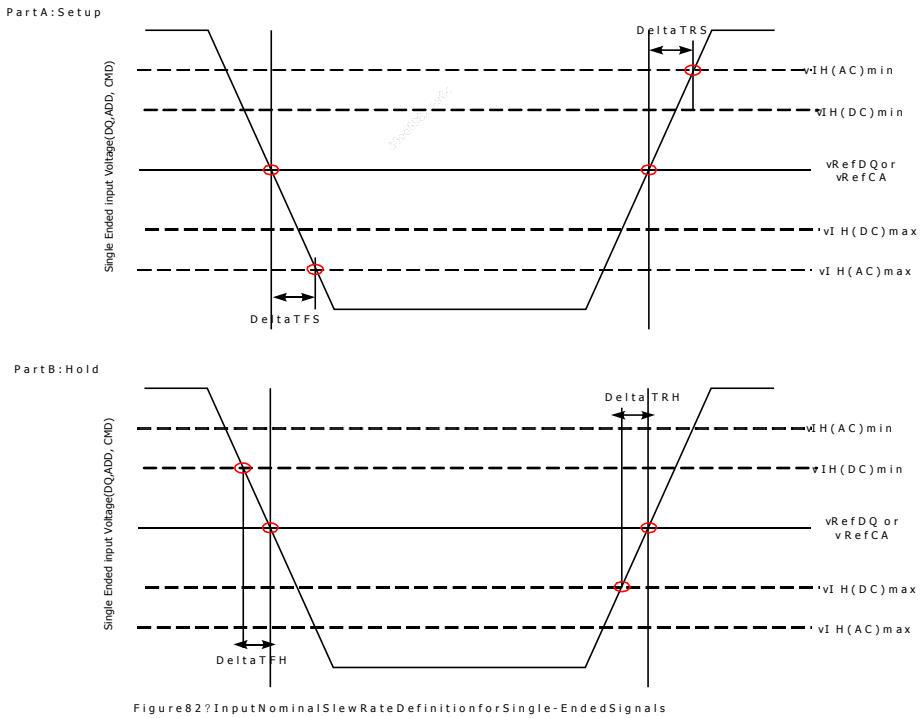


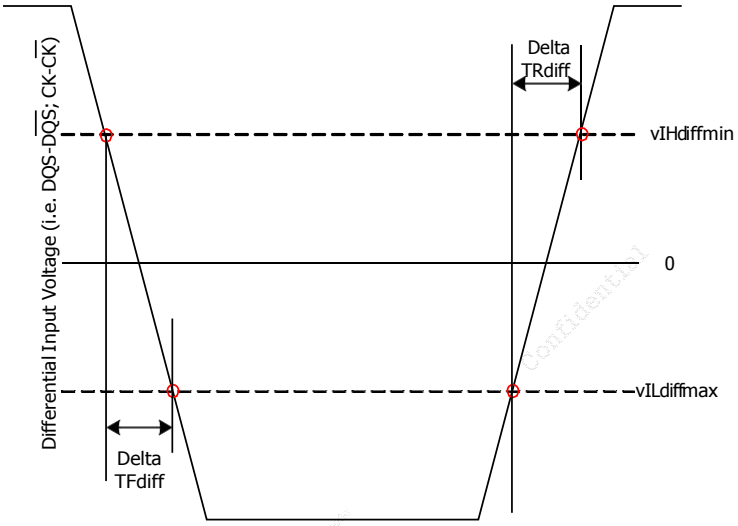
Figure82?InputNominalSlewRateDefinitionforSingle-EndedSignals

5.5 Slew Rate Definitions for Differential Input Signals

Input slew rate for differential signals (CK, CK and DQS, DQS) are defined and measured as shown in Table and Figure .

Description	Measured		Defined by
	Min	Max	
Differential input slew rate for rising edge (CK-CK and DQS-DQS)	VILdiffmax	VIHdiffmin	VIHdiffmin-VILdiffmax / DeltaTRdiff
Differential input slew rate for falling edge (CK-CK and DQS-DQS)	VIHdiffmin	VILdiffmax	VIHdiffmin-VILdiffmax / DeltaTFdiff

Note:
The differential signal (i.e. CK-$\overline{CK}$ and DQS-$\overline{DQS}$) must be linear between these thresholds.



Differential Input Slew Rate Definition for DQS, DQS# and CK, CK#

6. AC and DC Output Measurement Levels

6.1 Single Ended AC and DC Output Levels

Table shows the output levels used for measurements of single ended signals.

Symbol	Parameter	800/900MHz & 1.0GHz	Unit	Notes
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V	
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V	
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V	
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V	1
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V	1

1. The swing of ± 0.1 x VDDQ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ / 2.

6.1.1 Differential AC and DC Output Levels

Below table shows the output levels used for measurements of differential signals.

Symbol		900MHz & .0GHz	Unit	Notes
VOHdiff (AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V	1
VOLdiff (AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V	1

1. The swing of ± 0.2 x VDDQ is based on approximately 50% of the static differential output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to VTT = VDDQ/2 at each of the differential outputs.

6.2 Single Ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOL(AC) and VOH(AC) for single ended signals as shown in Table and Figure.

Description			Defined by
Single ended output slew rate for rising edge	VOL(AC)	VOH(AC)	$\frac{VOH(AC)-VOL(AC)}{DeltaTRse}$
Single ended output slew rate for falling edge	VOH(AC)	VOL(AC)	$\frac{VOH(AC)-VOL(AC)}{DeltaTFse}$

Note:
Output slew rate is verified by design and characterisation, and may not be subject to production test.

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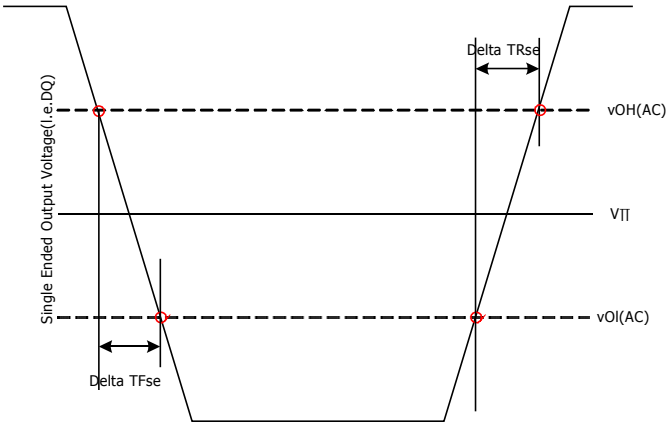
Single Ended Output Slew Rate Definition



Single Ended Output Slew Rate Definition

Output Slew Rate (single-ended)

Parameter		Hz		Units
			Max	
Single-ended Output Slew Rate	SRQse	2.5	5	V/ns

***** For Ron = RZQ/7 setting**

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6.3 Differential Output Slew Rate

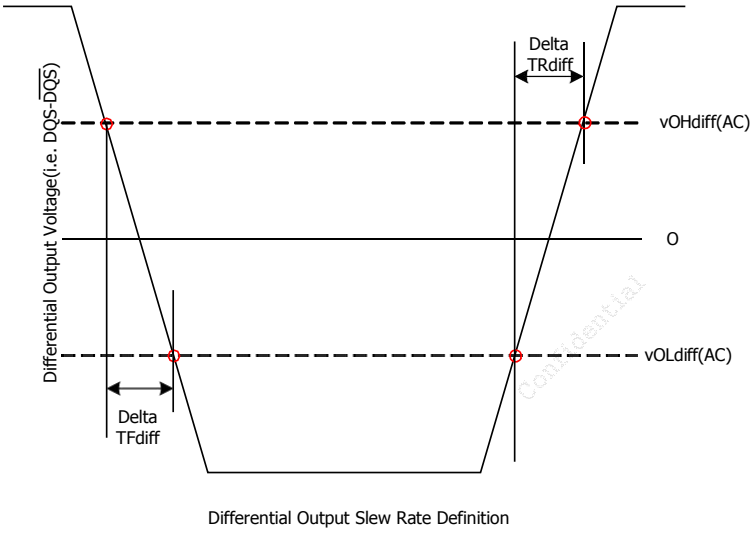
With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff (AC) and VOHdiff (AC) for differential signals as shown in Table and Figure .

Differential Output Slew Rate Definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	VOLdiff (AC)	VOHdiff (AC)	VOHdiff (AC)-VOLdiff (AC) DeltaTRdiff
Differential output slew rate for falling edge	VOHdiff (AC)	VOLdiff (AC)	VOHdiff (AC)-VOLdiff (AC) DeltaTFdiff

Note:

Output slew rate is verified by design and characterization, and may not be subject to production test.



Differential Output Slew Rate Definition

Differential Output Slew Rate

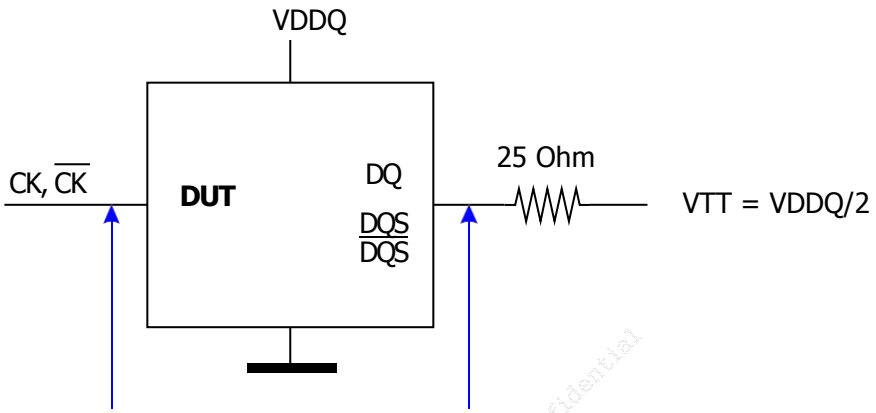
Parameter	Symbol	800/900MHz & 1.0GHz		Units
		Min	Max	
Differential Output Slew Rate	SRQdiff	5	10	V/ns

*****For Ron = RZQ/7 setting**

6.4 Reference Load for AC Timing and Output Slew Rate

Figure represents the effective reference load of 25 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.



Reference Load for AC Timing and Output Slew Rate

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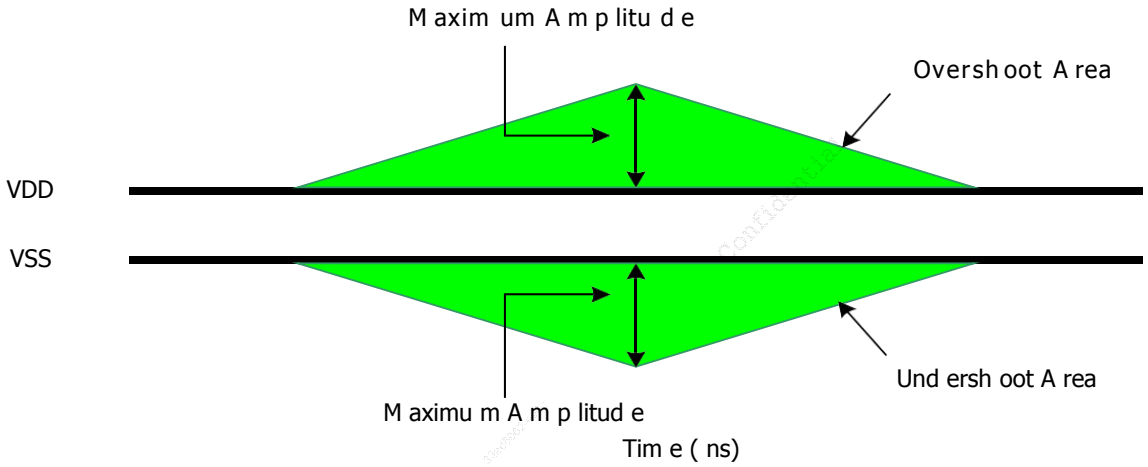
7. Overshoot and Undershoot Specifications

7.1 Address and Control Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Address and Control Pins

Description	Specification		
	800MHz	900MHz	1.0GHz
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDD (See Figure)	0.33 V-ns	0.28 V-ns	0.27 V-ns
Maximum undershoot area below VSS (See Figure)	0.33 V-ns	0.28 V-ns	0.27 V-ns

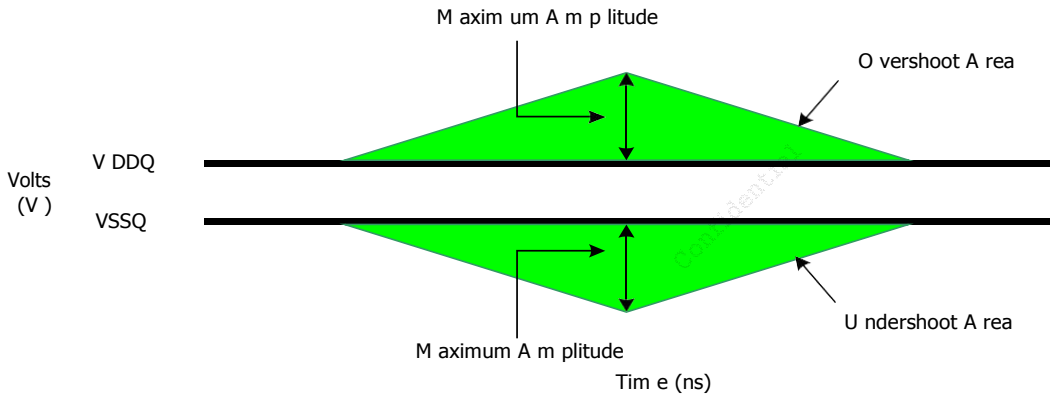


Address and Control Overshoot and Undershoot Definition

7.2 Clock, Data, Strobe and Mask Overshoot and Undershoot Specifications

AC Overshoot/Undershoot Specification for Clock, Data, Strobe and Mask

Description	Specification		
	800MHz	900MHz	1.0GHz
Maximum peak amplitude allowed for overshoot area (see Figure)	0.4V	0.4V	0.4V
Maximum peak amplitude allowed for undershoot area (see Figure)	0.4V	0.4V	0.4V
Maximum overshoot area above VDDQ (See Figure)	0.13 V-ns	0.11 V-ns	0.10 V-ns
Maximum undershoot area below VSSQ (See Figure)	0.13 V-ns	0.11 V-ns	0.10 V-ns



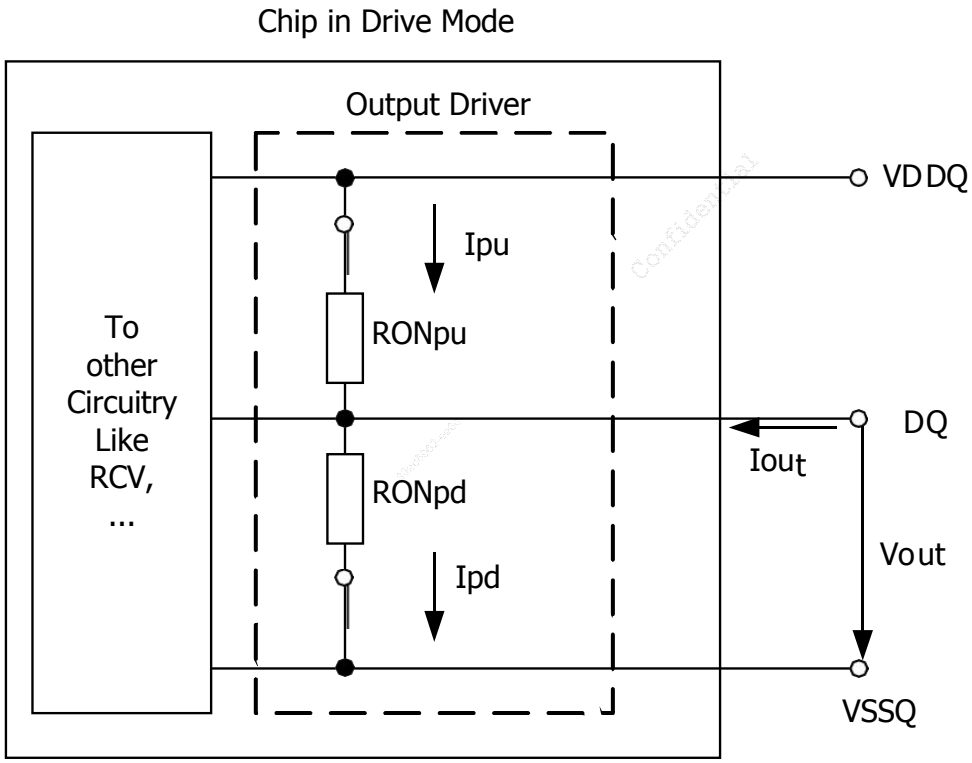
C lock, D ata Strob e and M ask O vershoot and U nders hoot D efinition

7.3 34 ohm Output Driver DC Electrical Characteristics

A functional representation of the output buffer is shown in Figure . Output driver impedance RON is defined by the value of the external reference resistor RZQ as follows:
RON34 = RZQ / 7 (nominal 34.3 W ±10% with nominal RZQ = 240 W ± 1%)
The individual pull-up and pull-down resistors (RONPu and RONPd) are defined as follows:

$$RON_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ **under the condition that RONPd is turned off**

$$RON_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ **under the condition that RONPu is turned off**



Output Driver: Definition of Voltages and Currents

Output Driver DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω ; entire operating temperature range; after proper ZQ calibration

RON_{Nom}	Resistor	V_{Out}	min	nom	max	Unit	Notes
34 Ω	RON_{34Pd}	V_{OLdc} = 0.2 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
	RON_{34Pu}	V_{OLdc} = 0.2 × V_{DDQ}	0.9	1.0	1.4	R_{ZQ}/7	1, 2, 3
		V_{OMdc} = 0.5 × V_{DDQ}	0.9	1.0	1.1	R_{ZQ}/7	1, 2, 3
		V_{OHdc} = 0.8 × V_{DDQ}	0.6	1.0	1.1	R_{ZQ}/7	1, 2, 3
Mismatch between pull-up and pull-down, MM_{PuPd}		V_{OMdc} 0.5 × V_{DDQ}	-10		+10	%	1, 2, 4

Notes:

1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.
2. The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.
3. Pull-down and pull-up outputdriver impedances are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd:
Measure RONPu and RONPd, both at 0.5 x VDDQ:

$$MM_{PuPd} = \frac{RON_{Pu} - RON_{Pd}}{RON_{Nom}} x100$$

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7.4 Output Driver Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .
DT = T - T (@calibration); DV= VDDQ - VDDQ (@calibration); VDD = VDDQ
dRONdT and dRONdV are not subject to production test but are verified by design and characterization.

Output Driver Sensitivity Definition

	min	max	unit
RONPU@ V_{OHdc}	0.6 - $dR_{ON}dTH$*| Δ T| - $dR_{ON}dVH$*| Δ V|	1.1 + $dR_{ON}dTH$*| Δ T| + $dR_{ON}dVH$*| Δ V|	RZQ/7
RON@ V_{OMdc}	0.9 - $dR_{ON}dTM$*| Δ T| - $dR_{ON}dVM$*| Δ V|	1.1 + $dR_{ON}dTM$*| Δ T| + $dR_{ON}dVM$*| Δ V|	RZQ/7
RONPD@ V_{OLdc}	0.6 - $dR_{ON}dTL$*| Δ T| - $dR_{ON}dVL$*| Δ V|	1.1 + $dR_{ON}dTL$*| Δ T| + $dR_{ON}dVL$*| Δ V|	RZQ/7

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
$dR_{ON}dTM$	0	1.5	%/°C
$dR_{ON}dVM$	0	0.15	%/mV
$dR_{ON}dTL$	0	1.5	%/°C

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$dR_{ON}dVL$	0	TBD	%/mV

Output Driver Voltage and Temperature Sensitivity

	min	max	unit
$dR_{ON}dTH$	0	1.5	%/°C
$dR_{ON}dVH$	0	TBD	%/mV

These parameters may not be subject to production test. They are verified by design and characterization.

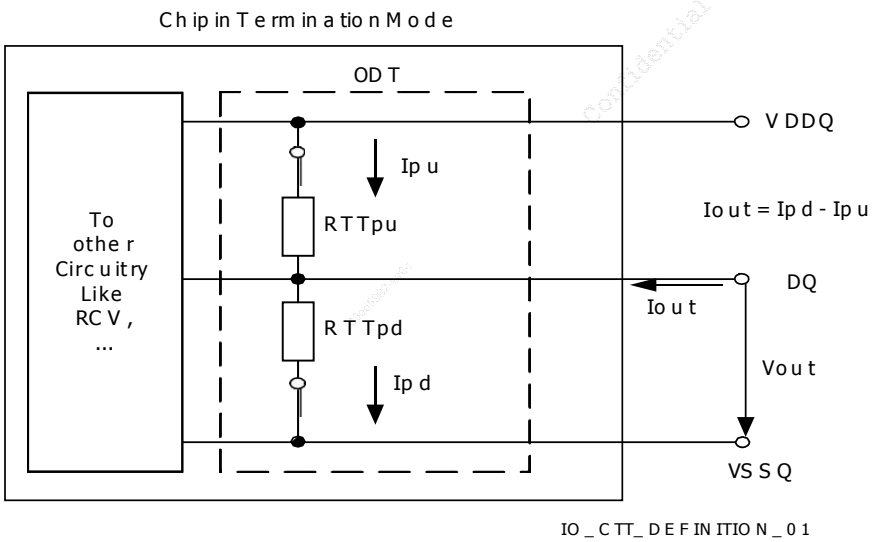
7.5 On-Die Termination (ODT) Levels and I-V Characteristics

7.5.1 On-Die Termination (ODT) Levels and I-V Characteristics

On-Die Termination effective resistance RTT is defined by bits A9, A6 and A2 of the MR1 Register.
ODT is applied to the DQ, DM, DQS/$\overline{DQS}$ and TDQS/$\overline{TDQS}$ (x8 devices only) pins.
A functional representation of the on-die termination is shown in Figure . The individual pull-up and pull-down resistors (RTTPu and RTTPd) are defined as follows:

$$RTT_{Pu} = \frac{V_{DDQ} - V_{Out}}{|I_{Out}|}$$ under the condition that RTTPd is turned off

$$RTT_{Pd} = \frac{V_{Out}}{|I_{Out}|}$$ under the condition that RTTPu is turned off



On-Die Termination: Definition of Voltages and Currents

7.5.2 ODT DC Electrical Characteristics

A below table provides an overview of the ODT DC electrical characteristics. The values for RTT60Pd120, RTT60Pu120, RTT120Pd240, RTT120Pu240, RTT40Pd80, RTT40Pu80, RTT30Pd60, RTT30Pu60, RTT20Pd40, RTT20Pu40 are not specification requirements, but can be used as design guide lines:

ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 0	120 Ω	$RTT_{120Pd240}$	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
		$RTT_{120Pu240}$	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.9	1.00	1.4	R_{ZQ}	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.6	1.00	1.1	R_{ZQ}	1) 2) 3) 4)
		RTT_{120}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/2$	1) 2) 5)
0, 0, 1	60 Ω	$RTT_{60Pd120}$	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1) 2) 3) 4)
		$RTT_{60Pu120}$	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/2$	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/2$	1) 2) 3) 4)
		RTT_{60}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/4$	1) 2) 5)

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ODT DC Electrical Characteristics, assuming R_{ZQ} = 240 Ω +/- 1% entire operating temperature range; after proper ZQ calibration

MR1 A9, A6, A2	*RTT*	Resistor	V_{Out}	min	nom	max	Unit	Notes
0, 1, 1	40 Ω	RTT_{40Pd80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/3$	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/3$	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/3$	1) 2) 3) 4)
		RTT_{40Pu80}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/3$	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/3$	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/3$	1) 2) 3) 4)
		RTT_{40}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/6$	1) 2) 5)
1, 0, 1	30 Ω	RTT_{30Pd60}	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/4$	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/4$	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/4$	1) 2) 3) 4)
		RTT_{30Pu60}	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/4$	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/4$	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/4$	1) 2) 3) 4)
		RTT_{30}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/8$	1) 2) 5)
1, 0, 0	20 Ω	RTT_{20Pd40}	V_{OLdc} $0.2 \cdot V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/6$	1) 2) 3) 4)
			$0.5 \cdot V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/6$	1) 2) 3) 4)
			V_{OHdc} $0.8 \cdot V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/6$	1) 2) 3) 4)
		RTT_{20Pu40}	V_{OLdc} $0.2 \times V_{DDQ}$	0.9	1.00	1.4	$R_{ZQ}/6$	1) 2) 3) 4)
			$0.5 \times V_{DDQ}$	0.9	1.00	1.1	$R_{ZQ}/6$	1) 2) 3) 4)
			V_{OHdc} $0.8 \times V_{DDQ}$	0.6	1.00	1.1	$R_{ZQ}/6$	1) 2) 3) 4)
		RTT_{20}	$V_{IL(ac)}$ to $V_{IH(ac)}$	0.9	1.00	1.6	$R_{ZQ}/12$	1) 2) 5)
Deviation of V_M w.r.t. $V_{DDQ}/2$, DV_M				-5		+5	%	1) 2) 5) 6)

The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

The tolerance limits are specified under the condition that VDDQ = VDD and that VSSQ = VSS.

Pull-down and pull-up ODT resistors are recommended to be calibrated at 0.5 x VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.2 x VDDQ and 0.8 x VDDQ.

Not a specification requirement, but a design guide line.

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Measurement definition for RTT:

Apply VIH (ac) to pin under test and measure current I(VIH (ac)), then apply VIL (ac) to pin under test and measure current I(VIL (ac)) respectively.

$$RTT = \frac{V_{IH(ac)} - V_{IL(ac)}}{I_{(VIH(ac))} - I_{(VIL(ac))}}$$

Measurement definition for VM and DVM:

Measure voltage (VM) at test pin (midpoint) with no load:

$$\Delta V_M = \left(\frac{2 \bullet V_M}{V_{DDQ}} - 1 \right) \bullet 100$$

7.5.3 ODT Temperature and Voltage sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to Table and Table .

DT = T - T (@calibration); DV= VDDQ - VDDQ (@calibration); VDD = VDDQ

ODT Sensitivity Definition

	m		unit
RTT	0.9 - $dR_{TT}dT^*\lvert\Delta T\rvert$ - $dR_{TT}dV^*\lvert\Delta V\rvert$	1.6 + $dR_{TT}dT^*\lvert\Delta T\rvert$ + $dR_{TT}dV^*\lvert\Delta V\rvert$	RZQ/2,4,6,8,12

ODT Voltage and Temperature Sensitivity

			unit
$dR_{TT}dT$	0	1.5	%/°C
$dR_{TT}dV$	0	0.15	%/mV

These parameters may not be subject to production test. They are verified by design and characterization

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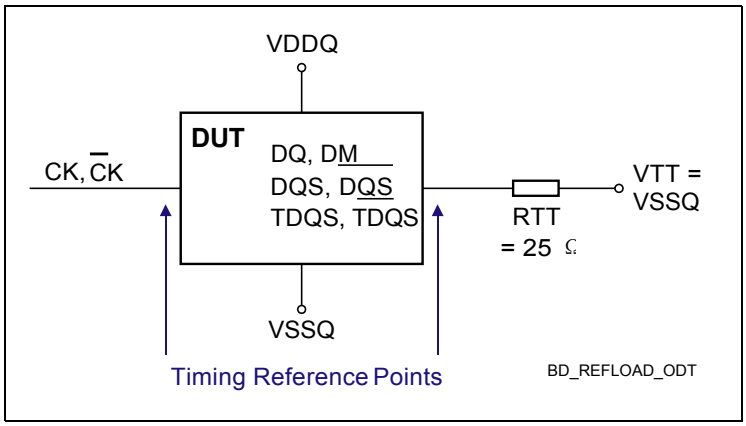
7.6 ODT Timing Definitions

7.6.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure .



Load

7.6.2 ODT Timing Reference

ODT Timing Definitions

Definitions for tAON, tAONPD, tAOF, tAOFPD and tADC are provided in the table and subsequent figures. Measurement reference settings are provided in the table.

ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure
t_{AON}	Rising edge of CK - CK defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure
t_{AONPD}	Rising edge of CK - CK with ODT being first registered high	Extrapolated point at VSSQ	Figure
t_{AOF}	Rising edge of CK - CK defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure
t_{AOFPD}	Rising edge of CK - CK with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure
t_{ADC}	Rising edge of CK - CK defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure

Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	V_{SW1} [V]	V_{SW2} [V]	Note
t_{AON}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AONPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOF}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{AOFPD}	$R_{ZQ}/4$	NA	0.05	0.10	
	$R_{ZQ}/12$	NA	0.10	0.20	
t_{ADC}	$R_{ZQ}/12$	$R_{ZQ}/2$	0.20	0.30	

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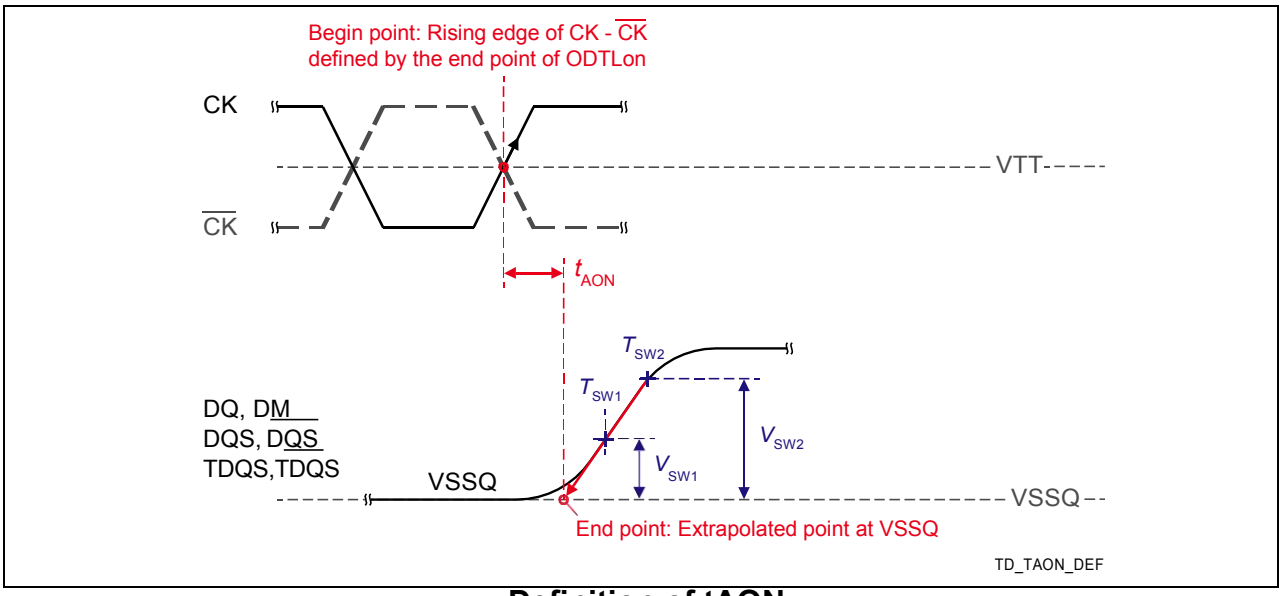
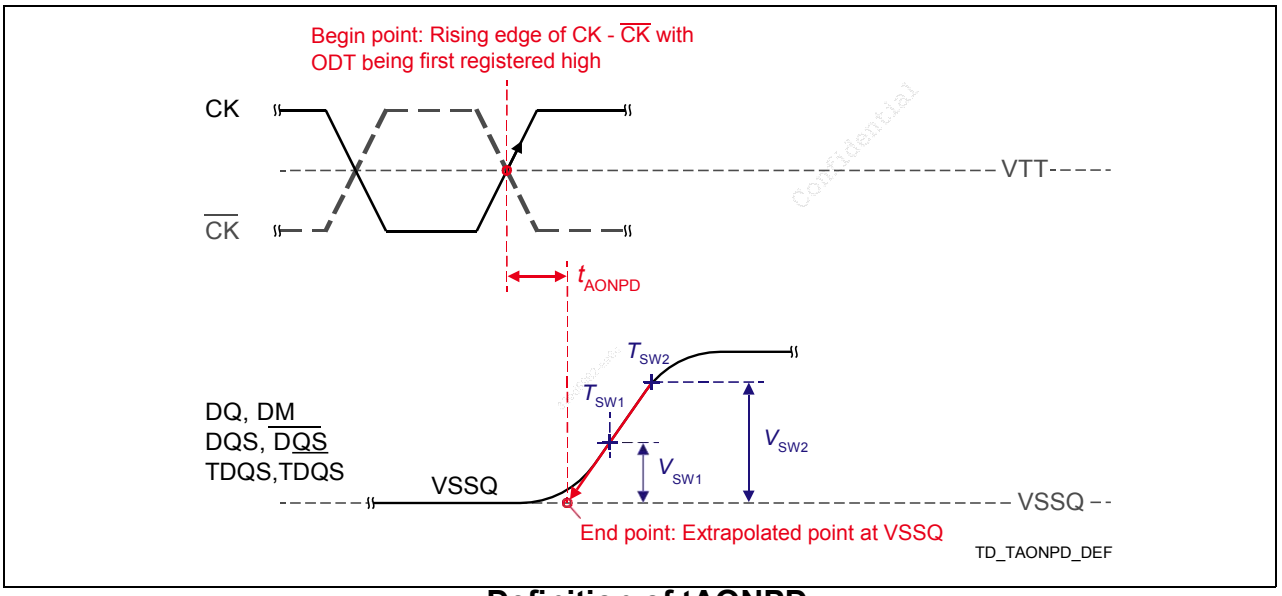
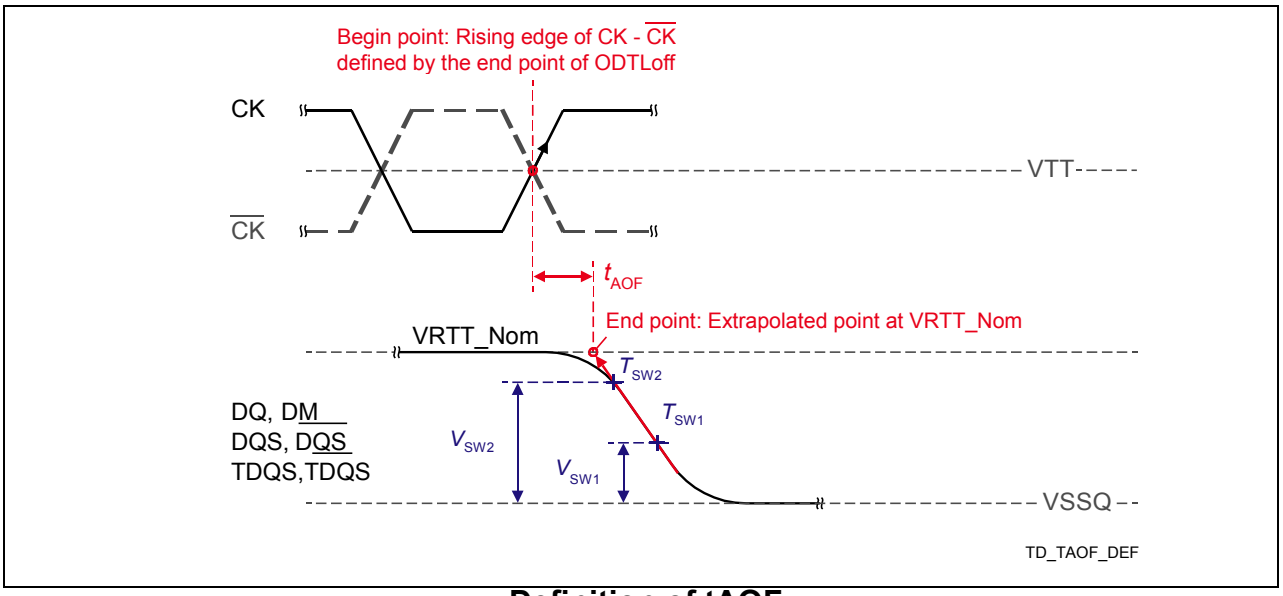


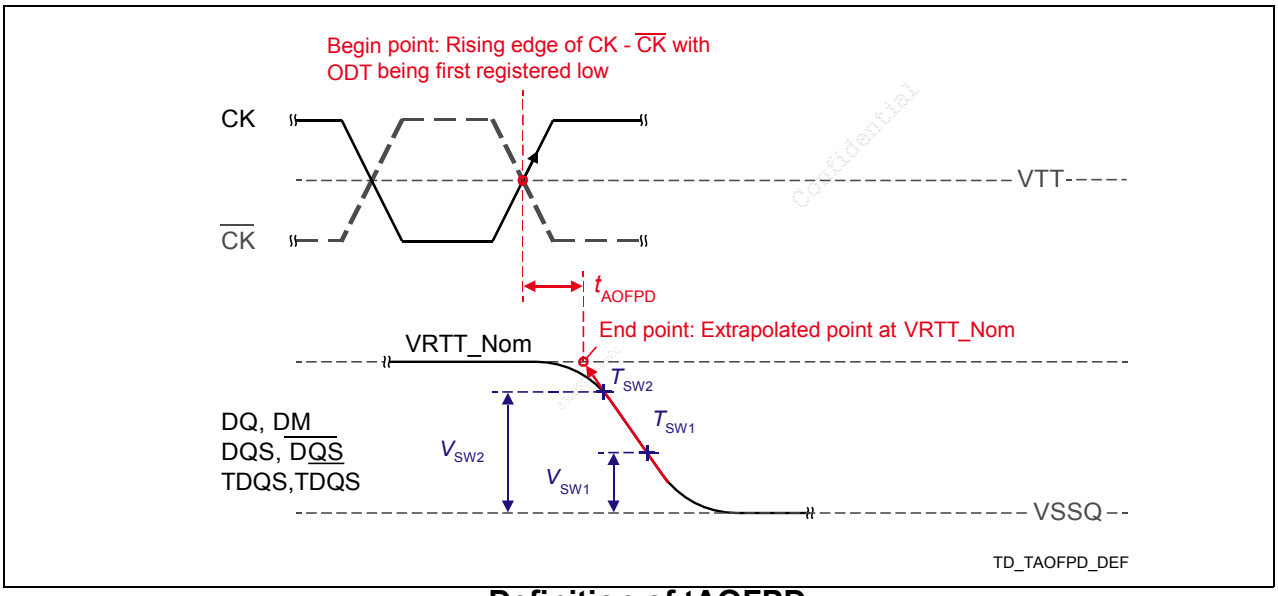
Definition of tAON



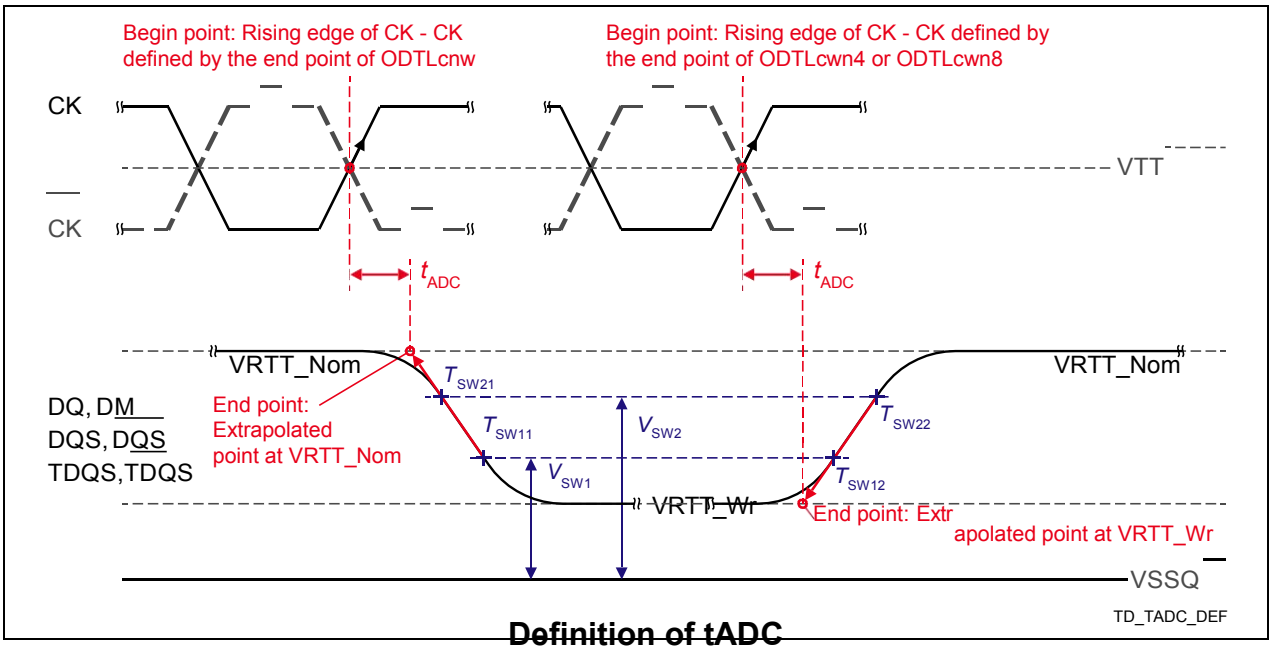
Definition of tAONPD



Definition of tAOF



Definition of tAOFPD



Definition of tADC

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8. IDD and IDDQ Specification Parameters and Test Conditions

8.1 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. Figure 1. shows the setup and test load for IDD and IDDQ measurements.

- IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET, IDD6TC and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR3 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 2. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD and IDDQ measurements, the following definitions apply:

- ”0” and “LOW” is defined as VIN <= $V_{ILAC(max)}$.
- ”1” and “HIGH” is defined as VIN >= $V_{IHAC(max)}$.
- “FLOATING” is defined as inputs are VREF - VDD/2.
- Timing used for IDD and IDDQ Measurement-Loop Patterns are provided in Table 1 on Page 39.
- Basic IDD and IDDQ Measurement Conditions are described in Table 2 on page 42.
- Detailed IDD and IDDQ Measurement-Loop Patterns are described in Table 3 on page 42 through Table 10 on page 47.
- IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  Qoff = 0_B (Output Buffer enabled in MR1);
  RTT_Nom = RZQ/6 (40 Ohm in MR1);
  RTT_Wr = RZQ/2 (120 Ohm in MR2);
  TDQS Feature disabled in MR1
- Attention: The IDD and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, LOW, LOW, LOW}
- Define $\overline{D}$ = {$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$}:= {HIGH, HIGH, HIGH, HIGH}

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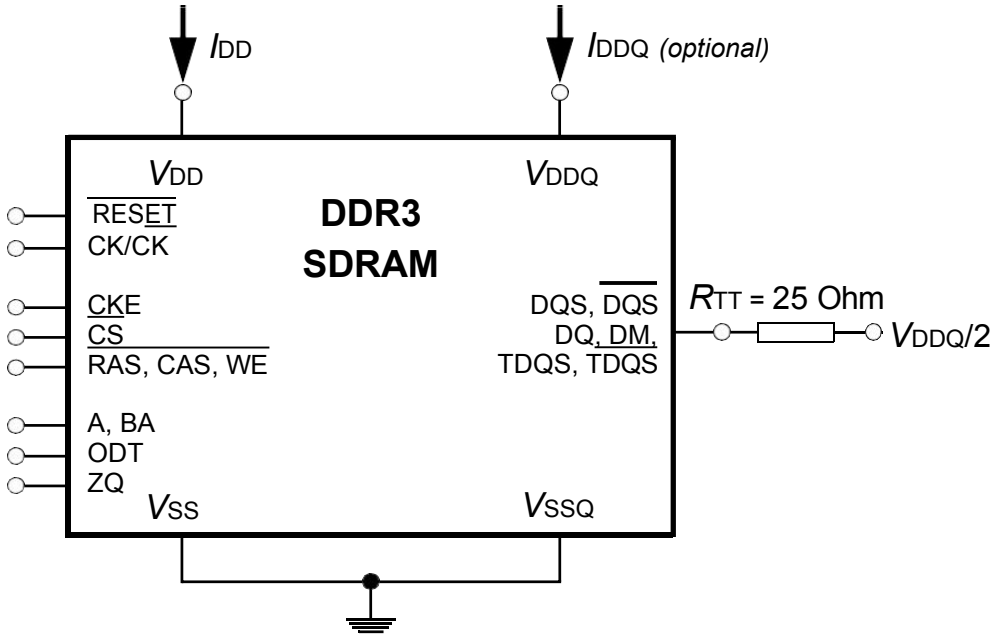

Figure 1 - Measurement Setup and Test Load for IDD and IDDQ (optional) Measurements
[Note: DIMM level Output test load condition may be different from above]

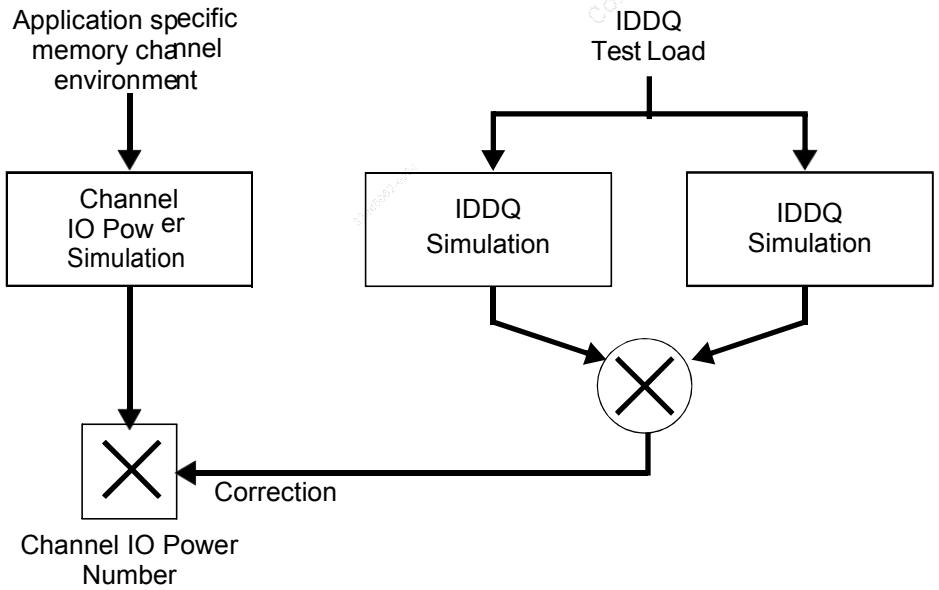

Figure 2 - Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement

Table 1 -Timings used for IDD and IDDQ Measurement-Loop Patterns

Symbol		800MHz	900MHz	1.0GHz	Unit
t_{CK}		1.25	1.1	1.0	ns
CL		10	11	12	nCK
n_{RCD}		12	13	15	nCK
n_{RC}		42	47	52	nCK
n_{RAS}		30	34	38	nCK
n_{RP}		12	13	15	nCK
n_{FAW}	x16	32	36	40	nCK
n_{RRD}	x16	6	6	6	nCK
n_{RFC}- 2 Gb		128	145	160	nCK

Table 2 -Basic IDD and IDDQ Measurement Conditions

Symbol	
I_{DD0}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, CL: see Table 1 on page 39; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling according to Table 3 on page 42; Data IO: FLOATING; DM: stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3 on page 42); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 3 on page 42
I_{DD1}	Operating One Bank Active-Precharge Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 1 on page 39; BL: 8[a)]; AL: 0; $\overline{CS}$: High between ACT, RD and PRE; Command, Address; Bank Address Inputs, Data IO : partially toggling according to Table 4 on page 43; DM: stable at 0; Bank Activity: Cycling with on bank active at a time: 0,0,1,1,2,2,... (see Table 4 on page 43); Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 4 page 43
I_{DD2N}	Precharge Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a)]; AL: 0; $\overline{CS}$: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 44

I_{DD2NT}	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 6 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: toggling according to Table 6 on page 44; Pattern Details: see Table 6 on page 44
I_{DDQ2NT} (optional)	Precharge Standby ODT IDDQ Current Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
I_{DD2P0}	Precharge Power-Down Current Slow Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit[c]
I_{DD2P1}	Precharge Power-Down Current Fast Exit CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit[c]
I_{DD2Q}	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DD3N}	Active Standby Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling according to Table 5 on page 44; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 5 on page 44
I_{DD3P}	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: FLOATING; DM: stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0
I_{DDQ4R} (optional)	Operating Burst Read IDDQ Current Same definition like for IDD4R, however measuring IDDQ current instead of IDD current

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I_{DD4R}	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling according to Table 7 on page 45; Data IO: seamless read data burst with different data between one burst and the next one according to Table 7 on page 45; DM: stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...(see Table 7 on page 45); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 7 on page 45
I_{DD4W}	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling according to Table 8 on page 45; Data IO: seamless read data burst with different data between one burst and the next one according to Table 8 on page 45; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...(see Table 8 on page 45); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at HIGH; Pattern Details: see Table 8 on page 45
I_{DD5B}	Burst Refresh Current CKE: High; External clock: On; tCK, CL, nRFC: see Table 1 on page 38; BL: 8[a]; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling according to Table 9 on page 45; Data IO: FLOATING; DM: stable at 0; Bank Activity: REF command every nREF (see Table 9 on page 45); Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details: see Table 9 on page 45
I_{DD6}	Self-Refresh Current: Normal Temperature Range T_{CASE}: 0 - 85 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and CK: LOW; CL: see Table 1 on page 4; BL: 8[a]; AL: 0; CS, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6ET}	Self-Refresh Current: Extended Temperature Range (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Disabled[d];Self-Refresh Temperature Range (SRT): Extended[e]; CKE: Low; External clock: Off; CK and CK: LOW; CL: see Table 1 on page 4; BL: 8[a]; AL: 0; CS, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING
I_{DD6TC}	Auto Self-Refresh Current (optional)[f] T_{CASE}: 0 - 95 °C; Auto Self-Refresh (ASR): Enabled[d];Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and CK: LOW; CL: see Table 1 on page 39; BL: 8[a]; AL: 0; CS, Command, Address, Bank Address Inputs, Data IO: FLOATING; DM: stable at 0; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: FLOATING

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I_{DD7}	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, NRRD, nFAW, CL: see Table 1 on page 39; BL: 8[a)]; AL: CL-1; $\overline{CS}$: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling according to Table 10 on page 47; Data IO: read data burst with different data between one burst and the next one according to Table 10 on page 47; DM: stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1,...7) with different addressing, wee Table 10 on page 47; Output Buffer and RTT: Enabled in Mode Registers[b)]; ODT Signal: stable at 0; Pattern Details: see Table 10 on page 47

a) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
b) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
c) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12 = 1B for Fast Exit
d) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
e) Self-Refresh Temperature Range (SRT): set MR2 A7 = 0B for normal or 1B for extended temperature range
f) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device

Table 3 - IDD0 Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	nd mma o	CS	RA S	CA S	WE	ODT	:0] A [2 B	:11] A[15	] A[1 0	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	C ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1. 4 until nRAS - 1, truncate if necess ary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1. 4 until nRC - 1, truncate if necessar y												
			1*nRC+0	ACT	0	0	1	1	0	00	00	0	0	F	0	-
			...	repeat pattern 1...4 until 1*nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern 1...4 until 2*nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 4 - IDD1 Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRCD - 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	00	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary												
			1*nRC+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			1*nRC+1,2	D, D	1	0	0	0	0	0	00	0	0	F	0	-
			1*nRC+3,4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until nRC + nRCE - 1, truncate if necessary												
			1*nRC+nRCD	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			...	repeat pattern nRC + 1,...4 until nRC + nRAS - 1, truncate if necessary												
			1*nRC+nRAS	PRE	0	0	1	0	0	0	00	0	0	F	0	-
			...	repeat pattern nRC + 1,...4 until *2 nRC - 1, truncate if necessary												
		1	2*nRC	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	4*nRC	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	6*nRC	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	8*nRC	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	10*nRC	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	12*nRC	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	14*nRC	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

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Table 5 - IDD2N and IDD3N Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	1	1	1	0	0	0	0	0	F	0	-
			3	D	1	1	1	1	0	0	0	0	0	F	0	-
		1	4-7	repeat Sub-Loop 0, use BA[2:0] = 1 instead												
		2	8-11	repeat Sub-Loop 0, use BA[2:0] = 2 instead												
		3	12-15	repeat Sub-Loop 0, use BA[2:0] = 3 instead												
		4	16-19	repeat Sub-Loop 0, use BA[2:0] = 4 instead												
		5	20-23	repeat Sub-Loop 0, use BA[2:0] = 5 instead												
		6	24-17	repeat Sub-Loop 0, use BA[2:0] = 6 instead												
		7	28-31	repeat Sub-Loop 0, use BA[2:0] = 7 instead												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

Table 6 - IDD2NT and IDDQ2NT Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	D	1	0	0	0	0	0	0	0	0	0	0	-
			1	D	1	0	0	0	0	0	0	0	0	0	0	-
			2	D	1	0	0	0	0	0	0	0	0	F	0	-
			3	D	1	0	0	0	0	0	0	0	0	F	0	00000000
		1	4-7	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 1												
		2	8-11	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 2												
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 3												
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 4												
		5	20-23	repeat Sub-Loop 0, but ODT = 0 and BA[2:0] = 5												
		6	24-17	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 6												
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

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Table 7 - IDD4R and IDDQ24RMeasurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	RD	0	1	0	1	0	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	0	0	00	0	0	0	0	-
			2,3	D,D	1	1	1	1	0	0	00	0	0	0	0	-
			4	RD	0	1	0	1	0	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	00	0	0	F	0	-
			6,7	D,D	1	1	1	1	0	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

Table 8 - IDD4W Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	A[15]	CS	RAS	CAS	WE	ODT	A[11]	BA[2:0]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	WR	0	1	0	0	1	0	00	0	0	0	0	00000000
			1	D	1	0	0	0	1	0	00	0	0	0	0	-
			2,3	D,D	1	1	1	1	1	0	00	0	0	0	0	-
			4	WR	0	1	0	0	1	0	00	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	00	0	0	F	0	-
			6,7	D,D	1	1	1	1	1	0	00	0	0	F	0	-
		1	8-15	repeat Sub-Loop 0, but BA[2:0] = 1												
		2	16-23	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	24-31	repeat Sub-Loop 0, but BA[2:0] = 3												
		4	32-39	repeat Sub-Loop 0, but BA[2:0] = 4												
		5	40-47	repeat Sub-Loop 0, but BA[2:0] = 5												
		6	48-55	repeat Sub-Loop 0, but BA[2:0] = 6												
		7	56-63	repeat Sub-Loop 0, but BA[2:0] = 7												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to WR Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Write Command. Outside burst operation, DQ signals are FLOATING.

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Table 9 - IDD5B Measurement-Loop Pattern[a)]

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	-
		1	1.2	D, D	1	0	0	0	0	0	00	0	0	0	0	-
			3,4	D, D	1	1	1	1	0	0	00	0	0	F	0	-
			5...8	repeat cycles 1...4, but BA[2:0] = 1												
			9...12	repeat cycles 1...4, but BA[2:0] = 2												
			13...16	repeat cycles 1...4, but BA[2:0] = 3												
			17...20	repeat cycles 1...4, but BA[2:0] = 4												
			21...24	repeat cycles 1...4, but BA[2:0] = 5												
			25...28	repeat cycles 1...4, but BA[2:0] = 6												
			29...32	repeat cycles 1...4, but BA[2:0] = 7												
		2	33...nRFC-1	repeat Sub-Loop 1, until nRFC - 1. Truncate, if necess ary.												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are FLOATING.
b) DQ signals are FLOATING.

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Table 10 - IDD7 Measurement-Loop Pattern[a)]

ATTENTION! Sub-Loops 10-19 have inverse A[6:3] Pattern and Data Pattern than Sub-Loops 0-9

CK, CK	CKE	Sub-Loop	Cycle Number	Command	CS	RAS	CAS	WE	ODT	BA[2:0]	A[15:11]	A[10]	A[9:7]	A[6:3]	A[2:0]	Data[b)]
toggling	Static High	0	0	ACT	0	0	1	1	0	0	00	0	0	0	0	-
			1	RDA	0	1	0	1	0	0	00	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	00	0	0	0	0	-
			...	repeat above D Command until nRRD - 1												
		1	nRRD	ACT	0	0	1	1	0	1	00	0	0	F	0	-
			nRRD+1	RDA	0	1	0	1	0	1	00	1	0	F	0	00110011
			nRRD+2	D	1	0	0	0	0	1	00	0	0	F	0	-
			...	repeat above D Command until 2* nRRD - 1												
		2	2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 2												
		3	3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 3												
		4	4*nRRD	D	1	0	0	0	0	3	00			0	F	0	-
			...	Assert and repeat above D Command until nFAW - 1, if necessary												
		5	nFAW	repeat Sub-Loop 0, but BA[2:0] = 4												
		6	nFAW+nRRD	repeat Sub-Loop 1, but BA[2:0] = 5												
		7	nFAW+2*nRRD	repeat Sub-Loop 0, but BA[2:0] = 6												
		8	nFAW+3*nRRD	repeat Sub-Loop 1, but BA[2:0] = 7												
		9	nFAW+4*nRRD	D	1	0	0	0	0	7	00	0	0	F	0	-
			...	Assert and repeat above D Command until 2* nFAW - 1, if necessary												
		10	2*nFAW+0	ACT	0	0	1	1	0	0	00	0	0	F	0	-
			2*nFAW+1	RDA	0	1	0	1	0	0	00	1	0	F	0	00110011
			2&nFAW+2	D	1	0	0	0	0	0	00	0	0	F	0	-
				Repeat above D Command until 2* nFAW + nRRD - 1												
		11	2*nFAW+nRRD	ACT	0	0	1	1	0	1	00	0	0	0	0	-
			2*nFAW+nRRD+1	RDA	0	1	0	1	0	1	00	1	0	0	0	00000000
			2&nFAW+nRRD+2	D	1	0	0	0	0	1	00	0	0	0	0	-
				Repeat above D Command until 2* nFAW + 2* nRRD - 1												
		12	2*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 2												
		13	2*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 3												
		14	2*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 3* nFAW - 1, if necessary												
		15	3*nFAW	repeat Sub-Loop 10, but BA[2:0] = 4												
		16	3*nFAW+nRRD	repeat Sub-Loop 11, but BA[2:0] = 5												
		17	3*nFAW+2*nRRD	repeat Sub-Loop 10, but BA[2:0] = 6												
		18	3*nFAW+3*nRRD	repeat Sub-Loop 11, but BA[2:0] = 7												
		14	3*nFAW+4*nRRD	D	1	0	0	0	0	0	00	0	0	0	0	-
				Assert and repeat above D Command until 4* nFAW - 1, if necessary												

a) DM must be driven LOW all the time. DQS, $\overline{DQS}$ are used according to RD Commands, otherwise FLOATING.
b) Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are FLOATING.

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8.2 IDD Specifications

IDD values are for full operating range of voltage and temperature unless otherwise noted.

I_{DD} Specification

Speed Grade Bin	800MHz	900MHz	1.0GHz	Unit	Notes
Symbol	Max.	Max.	Max.		
I_{DD0}	65	70	80	mA	
I_{DD1}	80	85	95	mA	
I_{DD2N}	30	35	40	mA	
I_{DD2P0}	10	10	12	mA	
I_{DD2P1}	20	20	22	mA	
I_{DD2Q}	30	35	40	mA	
I_{DD3N}	42	45	50	mA	
I_{DD3P}	20	22	25	mA	
I_{DD4R}	155	170	185	mA	
I_{DD4W}	165	180	200	mA	
I_{DD5}	165	180	200	mA	
I_{DD6}	10	10	12	mA	
I_{DD7}	190	210	230	mA	

*IDD Values can be slightly changed when above table is updated.

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9. Input/Output Capacitance

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Input/output capacitance (DQ, DM, DQS, DQS, TDQS, TDQS)	C_{IO}	1.5	2.3	TBD	TBD	TBD	TBD	pF	1,2,3
Input capacitance, CK and $\overline{CK}$	C_{CK}	0.8	1.4	TBD	TBD	TBD	TBD	pF	2,3
Input capacitance delta CK and CK	C_{DCK}	0	0.15	TBD	TBD	TBD	TBD	pF	2,3,4
Input capacitance (All other input-only pins)	C_I	0.75	1.3	TBD	TBD	TBD	TBD	pF	2,3,6
Input capacitance delta, DQS and DQS	C_{DDQS}	0	0.15	TBD	TBD	TBD	TBD	pF	2,3,5
Input capacitance delta (All CTRL input-only pins)	C_{DI_CTRL}	-0.4	0.2	TBD	TBD	TBD	TBD	pF	2,3,7,8
Input capacitance delta (All ADD/CMD input-only pins)	$C_{DI\_ADD\_CMD}$	-0.4	0.4	TBD	TBD	TBD	TBD	pF	2,3,9,10
Input/output capacitance delta (DQ, DM, DQS, $\overline{DQS}$)	C_{DIO}	-0.5	0.3	TBD	TBD	TBD	TBD	pF	2,3,11

Notes:

1. Although the DM, TDQS and $\overline{TDQS}$ pins have different functions, the loading matches DQ and DQS.
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147("PROCEDURE FOR MEASURING INPUT CAPACITANCE USING A VECTOR NETWORK ANALYZER(VNA)") with VDD, VDDQ, VSS,VSSQ applied and all other pins floating (except the pin under test, CKE, $\overline{RESET}$ and ODT as necessary). VDD=VDDQ=1.5V, VBIAS=VDD/2 and on-die termination off.
3. This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here
4. Absolute value of C_{CK}-$C_{\overline{CK}}$.
5. The minimum C_{CK} will be equal to the minimum C_I.
6. Input only pins include: ODT, CS, CKE, A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$.
7. CTRL pins defined as ODT, CS and CKE.
8. $C_{DI\_CTRL}=C_I(CNTL) - 0.5 * C_I(CLK) + C_I(\overline{CLK})$)
9. ADD pins defined as A0-A15, BA0-BA2 and CMD pins are defined as $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$.
10. $C_{DI\_ADD\_CMD}=C_I(ADD\_CMD) - 0.5*(C_I(CLK)+C_I(\overline{CLK}))$
11. $C_{DIO}=C_{IO}(DQ) - 0.5*(C_{IO}(DQS)+C_{IO}(\overline{DQS}))$

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10. Standard Speed Bins

DDR3 SDRAM Standard Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

800MHz Speed Bins

For specific Notes See "11. Electrical Characteristics and AC Timing" on page 71.

Speed Bin			800MHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	12.5	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	—	ns	
PRE command period		t_{RP}	15	—	ns	
ACT to ACT or REF command period		t_{RC}	51.25	—	ns	
ACT to PRE command period		t_{RAS}	37.5	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,4,6
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,6
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,6
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,6
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,6
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,6
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,6
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 10	CWL = 5,6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,6
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4
CL = 11	CWL = 5,6,7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4
Supported CL Settings			5,6, 7,8, 9,10,11		n_{CK}	
Supported CWL Settings			5, 6, 7,8		n_{CK}	

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900MHz Speed Bins

For specific Notes See "11. Electrical Characteristics and AC Timing" on page 71.

Speed Bin			900MHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	13.2	20	ns	
ACT to internal read or write delay time		t_{RCD}	15.4	—	ns	
PRE command period		t_{RP}	15.4	—	ns	
ACT to ACT or REF command period		t_{RC}	50.6	—	ns	
ACT to PRE command period		t_{RAS}	37.4	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,4,7
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,7
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,7
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,7
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,7
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,7
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4,7
CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL=8	$t_{CK(AVG)}$	1.25	1.5		1,2,3,4,7
	CWL = 9	$t_{CK(AVG)}$	1.1	1.25	ns	1,2,3,4
Supported CL Settings			5,6, 7,8, 9,10,11		n_{CK}	
Supported CWL Settings			5, 6, 7,8,9		n_{CK}	

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1.0GHzMHz Speed Bins

For specific Notes See "11. Electrical Characteristics and AC Timing" on page 71.

Speed Bin			1.0GHz		Unit	Note
Parameter		Symbol	min	max		
Internal read command to first data		t_{AA}	12.0	20	ns	
ACT to internal read or write delay time		t_{RCD}	15	-	ns	
PRE command period		t_{RP}	15	-	ns	
ACT to ACT or REF command period		t_{RC}	52	-	ns	
ACT to PRE command period		t_{RAS}	37	9 * tREFI	ns	
CL = 5	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,4,8
	CWL = 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 6	CWL = 5	$t_{CK(AVG)}$	2.5	3.3	ns	1,2,3,8
	CWL = 6	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	4
CL = 7	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,4,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	4
CL = 8	CWL = 5	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 6	$t_{CK(AVG)}$	1.875	2.5	ns	1,2,3,8
	CWL = 7	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4,8
CL = 9	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,4,8
	CWL = 8	$t_{CK(AVG)}$	Reserved		ns	1,2,3,4
CL = 10	CWL = 5, 6	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 7	$t_{CK(AVG)}$	1.5	1.875	ns	1,2,3,8
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,4
CL = 11	CWL = 5, 6, 7	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 8	$t_{CK(AVG)}$	1.25	1.5	ns	1,2,3,8
	CWL = 9	$t_{CK(AVG)}$	1.0	1.25	ns	1,2,3,5
CL = 12	CWL = 5, 6, 7,8	$t_{CK(AVG)}$	Reserved		ns	4
	CWL = 9	$t_{CK(AVG)}$	1.0	1.25	ns	1,2,3,5,8
Supported CL Settings			5,6,7,8,9,10,11,12		n_{CK}	
Supported CWL Settings			5,6,7,8,9		n_{CK}	

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Speed Bin Table Notes

Absolute Specification (T_{OPER}; V_{DDQ} = V_{DD} = 1.5V +/- 0.075 V);

Notes:

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK (AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK (AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK (AVG) [ns], rounding up to the next 'Supported CL'.
3. tCK(AVG).MAX limits: Calculate tCK (AVG) = tAA.MAX / CLSELECTED and round the resulting tCK (AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CLSE LECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and SPD information if and how this setting is supported.
6. Any 800MHz speed bin also supp orts functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any 900MHz speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any 1.0GHz speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. It is not a mandatory bin. Refer to supplier's data sheet and/or the DIMM SPD information.
10. If it's supported, the minimum tAA/tRCD/tRP that this device support is 13.125ns. Therefore, In Module application, tAA/tRCD/tRP should be programed with minimum supported values.

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11. Electrical Characteristics and AC Timing

Timing Parameters by Speed Bin

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns	6
Average Clock Period	tCK (avg)	See “10. Standard Speed Bins” on page 62.						ps	f
Average high pulse width	tCH (avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Average low pulse width	tCL (avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK (avg)	f
Absolute Clock Period	tCK (abs)	tCK(avg)min+tJIT(per)min						ps	
Absolute clock HIGH pulse width	tCH (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	25
Absolute clock LOW pulse width	tCL (abs)	0.43	-	0.43	-	0.43	-	tCK (avg)	26
Clock Period Jitter	JIT (per)	-70	70	-60	60	-40	40	ps	
Clock Period Jitter during DLL locking period	tJIT (per, lck)	-60	60	-50	50	-30	30	ps	
Cycle to Cycle Period Jitter	tJIT (cc)	140	140	130	130	TBD	TBD	ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT (cc, lck)	120	120	110	110	TBD	TBD	ps	
Duty Cycle jitter	tJIT (duty)	-	-	-	-	TBD	TBD	ps	
Cumulative error across 2 cycles	tERR (2per)	-103	103	-93	93	TBD	TBD	ps	
Cumulative error across 3 cycles	tERR (3per)	-122	122	-112	112	TBD	TBD	ps	
Cumulative error across 4 cycles	tERR (4per)	-136	136	-122	122	TBD	TBD	ps	
Cumulative error across 5 cycles	tERR (5per)	-147	147	-135	135	TBD	TBD	ps	
Cumulative error across 6 cycles	tERR (6per)	-155	155	-140	140	TBD	TBD	ps	
Cumulative error across 7 cycles	tERR (7per)	-163	163	-146	146	TBD	TBD	ps	
Cumulative error across 8 cycles	tERR (8per)	-169	169	-149	149	TBD	TBD	ps	
Cumulative error across 9 cycles	tERR (9per)	-175	175	-160	160	TBD	TBD	ps	

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Cumulative error across 10 cycles	tERR (10per)	-180	180	-165	165	TBD	TBD	ps	

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Cumulative error across 11 cycles	tERR (11per)	-184	184	-168	168	TBD	TBD	ps	
Cumulative error across 12 cycles	tERR (12per)	-188	188	-170	170	TBD	TBD	ps	
Cumulative error across n = 13, 14,.....49, 50 cycles	tERR (nper)	tERR(nper)min=(1+0.68ln(n))*JIT(per)min tERR(nper)max=(1+0.68ln(n))*JIT(per)max						ps	24
Data Timing									
DQS, DQS to DQ skew, per group, per access	tDQSQ	100	-	87	-	75	-	ps	13
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQ low-impedance time from CK, CK	tLZ (DQ)	-450	225	-400	200	-360	180	ps	13, 14, a
DQ high impedance time from CK, CK	tHZ (DQ)	-	225	-	200	-	180	ps	13, 14, a
Data setup time to DQS, DQS referenced to Vih (ac) / Vil (ac) levels	tDS (base)	10	-	0	-	-10	-	ps	d, 17
Data hold time from DQS, DQS referenced to Vih (dc) / Vil (dc) levels	tDH (base)	45	-	45	-	40	-	ps	d, 17
Data Strobe Timing									
DQS,DQS differential READ Preamble	tRPRE	0.9	Note	0.9	Note	0.9	TBD	tCK (avg)	13, 19 b
DQS, DQS differential READ Postamble	tRPST	0.3	Note	0.3	Note	0.3	TBD	tCK (avg)	11, 13, b
DQS, DQS differential output high time	tQSH	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, DQS differential output low time	tQSL	0.38	-	0.38	-	0.38	-	tCK (avg)	13, b
DQS, DQS differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK (avg)	
DQS, DQS differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK (avg)	
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-225	225	-180	180	-180	180	ps	13, a

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Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
DQS and DQS low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-450	225	-400	200	-360	180	ps	13, 14, a
DQS and DQS high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	225	-	200	-	180	ps	13, 14 a
DQS, DQS differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, DQS differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK (avg)	
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.3	0.3	tCK (avg)	c
DQS, DQS falling edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK (avg)	c
DQS, DQS falling edge hold time from CK, CK rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK (avg)	c
Command and Address Timing									
DLL locking time	tDLLK	512	-	512	-	512	-	nCK	
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-		e, 18
WRITE recovery time	tWR	16.3	-	15.6	-	15	-	ns	e
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK	
Mode Register Set command update delay	tMOD	max(12nCK,15ns)	-	max(12nCK,15ns)	-	max(12nCK,15ns	-		
ACT to internal read or write delay time	tRCD	16.3	-	15.6	-	15	-		e
PRE command period	tRP	16.3	-	15.6	-	15	-		e
ACT to ACT or REF command period	tRC	52.5	-	50	-	51	-		e
CAS to CAS command delay	tCCD	4	-	4	-	4	-	nCK	

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Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Auto precharge write recovery + precharge time	tDAL (min)	24	-	28	-	31	-	nCK	
End of MPR Read burst to MSR for MPR (exit)	tMPRR	1	-	1	-	1	-	nCK	22
ACTIVE to PRECHARGE command period	tRAS	37.5	-	35.6	-	34	-		e
ACTIVE to ACTIVE command period for 2KB page size	tRRD	7	-	7	-	7	-		e
Four activate window for 2KB page size	tFAW	42.5	-	41.1	-	40	-	ns	e
Command and Address setup time to CK, CK referenced to Vih (ac) / Vil (ac) levels	tIS (base)	45	-	35		25	-	ps	b, 16
Command and Address hold time from CK, CK referenced to Vih (dc) / Vil (dc) levels	tIH (base)	120	-	110	-	100	-	ps	b, 16
Calibration Timing									
Power-up and RESET calibration time	tZQinit	512	-	512	-	512	-	nCK	
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	nCK	
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	nCK	23
Reset Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-		
Self Refresh Timings									
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-	max(5nsCK, tRFC(min)+10ns)	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK	

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Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	tCKE(min)+1nCK	tCKE(min)+1nCK	-		

Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-	max(5nsCK, 10ns)	-		
Power Down Timings									
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	7	-	7	-	7	-		
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	MAX(10nC	MAX(K,24ns)	MAX(10nCK,24ns)	-	K,24 10nCns)	-		2
CKE minimum pulse width	tCKE	4	-	5	-	5	-		
Command pass disable delay	tCPDED						-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		15
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK	
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK	
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK	9

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Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR +1	-	WL+4+WR +1	-	WL+4+WR +1	-	nCK	10
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tW R/ tCK(avg))	-	WL+2+(tW R/ tCK(avg))	-	WL+2+(tW R/ tCK(avg))	-	nCK	9
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR +1	-	WL+2+WR +1	-	WL+2+WR +1	-	nCK	10
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	nCK	,
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
ODT Timings									
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK	
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK	
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	1	9	ns	
RTT turn-on	tAON	-225	225	-200	200	-175	175	ps	7, a
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	8, a
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK (avg)	a
Write Leveling Timings									

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First DQS/DQS rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	3

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Timing Parameters by Speed Bin (Continued)

Note: The following general notes from page 61 apply to Table : a

		800MHz		900MHz		1.0GHz			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**	**Notes**
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	3
Write leveling setup time from rising CK, CK crossing to rising DQS, DQS crossing	tWLS	170	-	130	-	120	-	ps	
Write leveling hold time from rising DQS, DQS crossing to rising CK, CK crossing	tWLH	170	-	130	-	120	-	ps	
Write leveling output delay	tWLO	0	9	0	9	0	9	ns	
Write leveling output error	tWLOE	0	2	0	2	0	2	ns	

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0.1 Jitter Notes

Specific Note a When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR (mper), act of the input clock, where 2 <= m <=12.(output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR-800 SDRAM has tERR (mper), act, min = -172 ps and tERR (mper), act, max =+ 193 ps, then t DQSCK, min (derated) = tDQSCK, min - tERR (mper), act, max = -400 ps - 193 ps = - 593 ps and tDQSCK, max (derated) = tDQSCK, max - tERR (mper), act, min = 400 ps+ 172 ps = + 572 ps. Similarly, tLZ (DQ) for DDR3-800 derates to tLZ (DQ), min (derated) = - 800 ps - 193 ps = - 993 ps and tLZ (DQ), max (derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!) Note that tERR (mper), act, min is the minimum measured value of tERR (nper) where 2 <= n <=12, and tERR (mper), act, max is the maximum measured value of tERR (nper) where 2 <= n <= 12

Specific Note b When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT (per), act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK (avg), act = 2500 ps, tJIT (per), act, min = - 72 ps and tJIT (per), act, max = + 93 ps, then tRPRE, min (derated) = tRPRE, min + tJIT (per), act, min = 0 .9 x tCK (avg), act + tJIT (per), act, min (derated) = tRPRE, min + tJIT (per), act, min = 0.9 x tCK (avg), act + tJIT (per), act, min = 0.9 x 2500 ps - 72 ps =+ 2178 ps. Similarly, tQH, min (derated) = tQH, min + tJIT (per), act, min = 0.38 x tCK (avg), act + tJIT (per), act, min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

Specific Note c These parameters are measured from a data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing to its respective clock signal (CK, CK) crossing. The values are not affected by the amount of clock jitter applied (i.e. tJIT (per), tJIT (cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

Specific Note d These parameters are measured from a data signal (DM(L/U), DQ(L/U)0, DQ(L/U)1, etc.) transition edge to its respective data strobe signal (DQS(L/U), $\overline{\text{DQS}}$(L/U)) crossing.

Specific Note e For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU {tPARAM [ns] / tCK (avg) [ns]}, which is in clock cycles, assuming all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU {tRP / tCK (avg)} = 6, i.e. 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

Specific Note f These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing holds at all times. (Min and max of SPEC values are to be used for calculations in Table .

Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register.
5. Value must be rounded-up to next higher integer value.
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
8. WR in clock cycles as programmed in MR0.
9. The maximum postamble is bound by tHZDQS (max)
10. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by t.b.d.
11. Value is only valid for RON34
12. Single ended signal parameter. Refer to chapter <t.b.d.> for definition and measurement method.
13. tREFI depends on TOPER
14. tIS (base) and tIH (base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ (DC). For input only pins except $\overline{RESET}$, VRef (DC) = VRefCA (DC). See "Address / Command Setup, Hold and Derating" on page 80.
15. tDS (base) and tDH (base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, VREF(DC) = VRefDQ (DC). For input only pins except $\overline{RESET}$, VRef (DC) = VRefCA (DC). See "Data Setup, Hold and Slew Rate Derating" on page 87..
16. Start of internal write transaction is definited as follows:
    For BL8 (fixed by MRS and on- the-fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (on- the- fly): Rising clock edge 4 clock cycles after WL.
    For BC4 (fixed by MRS): Rising clock edge 2 clock cycles after WL.
17. The maximum preamble is bound by tLZDQS (min)
18. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
19. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN (min) is satisfied, there are cases where additional time such as tXPDLL (min) is also required.
20. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
21. One ZQCS command can effectively correct a minimum of 0.5% (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdrifrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula.

$$\frac{ZQCorrection}{(Tsens \times Tdriftrate)+(VSens \times Vdriftrate)}$$

where TSens = max (dRTTdT, dRONdTM) and VSens = max (dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities. For example, if TSens = 1.5% / ^{o}C, VSens = 0.15% / mV, Tdriftrate = 1 ^{o}C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

$$\frac{0.5}{(1.5 \times 1)+(0.15 \times 15)} = 0.133 = 128ms$$

22. n = from 13 cycles to 50 cycles.
23. tCH (abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
24. tCL (abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
25. The tIS (base) AC150 specifications are adjusted from the tIS (base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mV - 150 mV) / 1 V/ns].

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Address / Command Setup, Hold and Derating

For all input signals the total tIS (setup time) and tIH (hold time) required is calculated by adding the data sheet tIS (base) and tIH (base) value (see Table 11) to the ΔtIS and ΔtIH derating value (see Table 12) respectively. Example: tIS (total setup time) = tIS (base) + ΔtIS

Setup (tIS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tIS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of Vil (ac) max. If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value (see Figure 4). If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 6).

Hold (tIH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of Vil (dc) max and the first crossing of $V_{REF(dc)}$. Hold (tIH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of Vih (dc) min and the first crossing of $V_{REF(dc)}$. If the actual signal is always later than the nominal slew rate line between shaded 'dc to $V_{REF(dc)}$ region', use nominal slew rate for derating value (see Figure 5). If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see Figure 6).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 14).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in Table 12, the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 11 - ADD/CMD Setup and Hold Base-Values for 1V/ns

unit [ps]	800MHz	900MHz	1.0GHz	reference
tIS (base)	45	35	TBD	$V_{IH/L(ac)}$
tIH (base)	120	110	TBD	$V_{IH/L(dc)}$
tIH(base)AC150	45 + 125	35 + 125	TBD + 125	$V_{IH/L(dc)}$

Note: - (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS slew rate)

- The tIS (base) AC150 specifications are adjusted from the tIS (base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the ear lier reference point [(175 mV - 150 mV) / 1 V/ns]

Table 12 - Derating values tIS/tIH - ac/dc based

AC175 Thresho																	
		CK,CK Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH	Δ tIS	Δ tIH
CMD / ADD Slew rate V/ns	2.0	88	50	88	50	88	50	96	58	104	66	112	74	120	84	128	100
	1.5	59	34	59	34	59	34	67	42	75	50	83	58	91	68	99	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	-2	-4	-2	-4	-2	-4	6	4	14	12	22	20	30	30	38	46
	0.8	-6	-10	-6	-10	-6	-10	2	-2	10	6	18	14	26	24	34	40
	0.7	-11	-16	-11	-16	-11	-16	-3	-8	5	0	13	8	21	18	29	34
	0.6	-17	-26	-17	-26	-17	-26	-9	-18	-1	-10	7	-2	15	8	23	24
	0.5	-35	-40	-35	-40	-35	-40	-27	-32	-19	-24	-11	-16	-2	-6	5	10
	0.4	-62	-60	-62	-60	-62	-60	-54	-52	-46	-44	-38	-36	-30	-26	-22	-10

Table 13 - Derating values tIS/tIH - ac/dc based

ΔtIS, ΔtIH derating in [ps] AC/DC based Alternate AC150 Threshold -> VIH (ac) = VREF (dc) + 150mV, VIL (ac) = VREF (dc) - 150mV																
		CK,CK Differential Slew Rate														
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH	ΔtIS	ΔtIH
CMD / ADD Slew rate V/ns	2.0	75	50	75	50	75	50	83	58	91	66	99	74	107	84	115	100
	1.5	50	34	50	34	50	34	58	42	66	50	74	58	82	68	90	84
	1.0	0	0	0	0	0	0	8	8	16	16	24	24	32	34	40	50
	0.9	0	-4	0	-4	0	-4	8	4	16	12	24	20	32	30	40	46
	0.8	0	-10	0	-10	0	-10	8	-2	16	6	24	14	32	24	40	40
	0.7	0	-16	0	-16	0	-16	8	-8	16	0	24	8	32	18	40	34
	0.6	-1	-26	-1	-26	-1	-26	7	-18	15	-10	23	-2	31	8	39	24
	0.5	-10	-40	-10	-40	-10	-40	-2	-32	6	-24	14	-16	22	-6	30	10
	0.4	-25	-60	-25	-60	-25	-60	-17	-52	-9	-44	-1	-36	7	-26	15	-10

Table 14 - Required time t_{VAC} above VIH (ac) {below VIL (ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} @ 175 mV [ps]		t_{VAC} @ 150 mV [ps]	
	min	max	min	max
> 2.0	75	-	175	-
2.0	57	-	170	-
1.5	50	-	167	-
1.0	38	-	163	-
0.9	34	-	162	-
0.8	29	-	161	-
0.7	22	-	159	-
0.6	13	-	155	-
0.5	0	-	150	-
< 0.5	0	-	150	-

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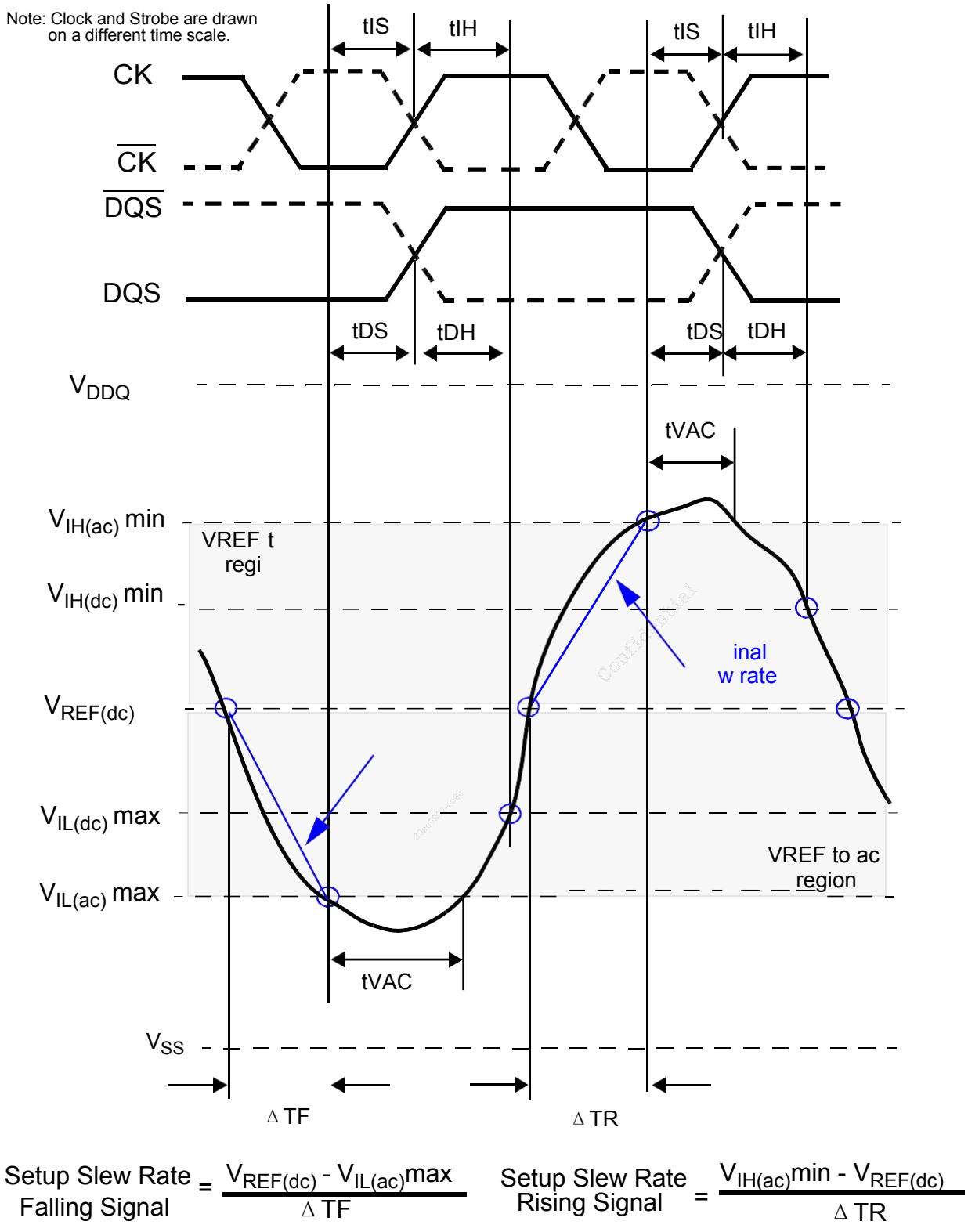

Figure 3 - Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

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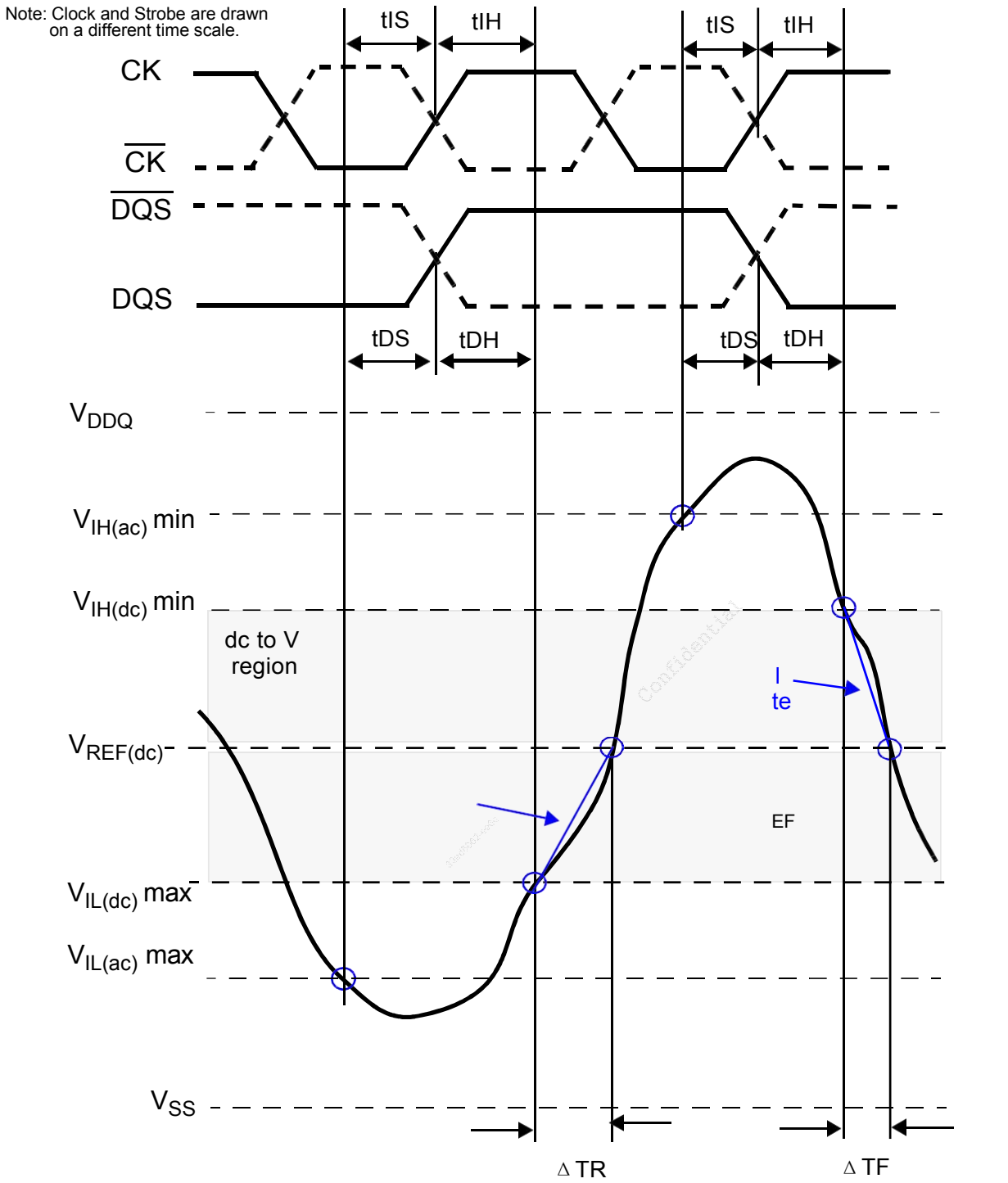

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta\,TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta\,TF}$$

Figure 4 - Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

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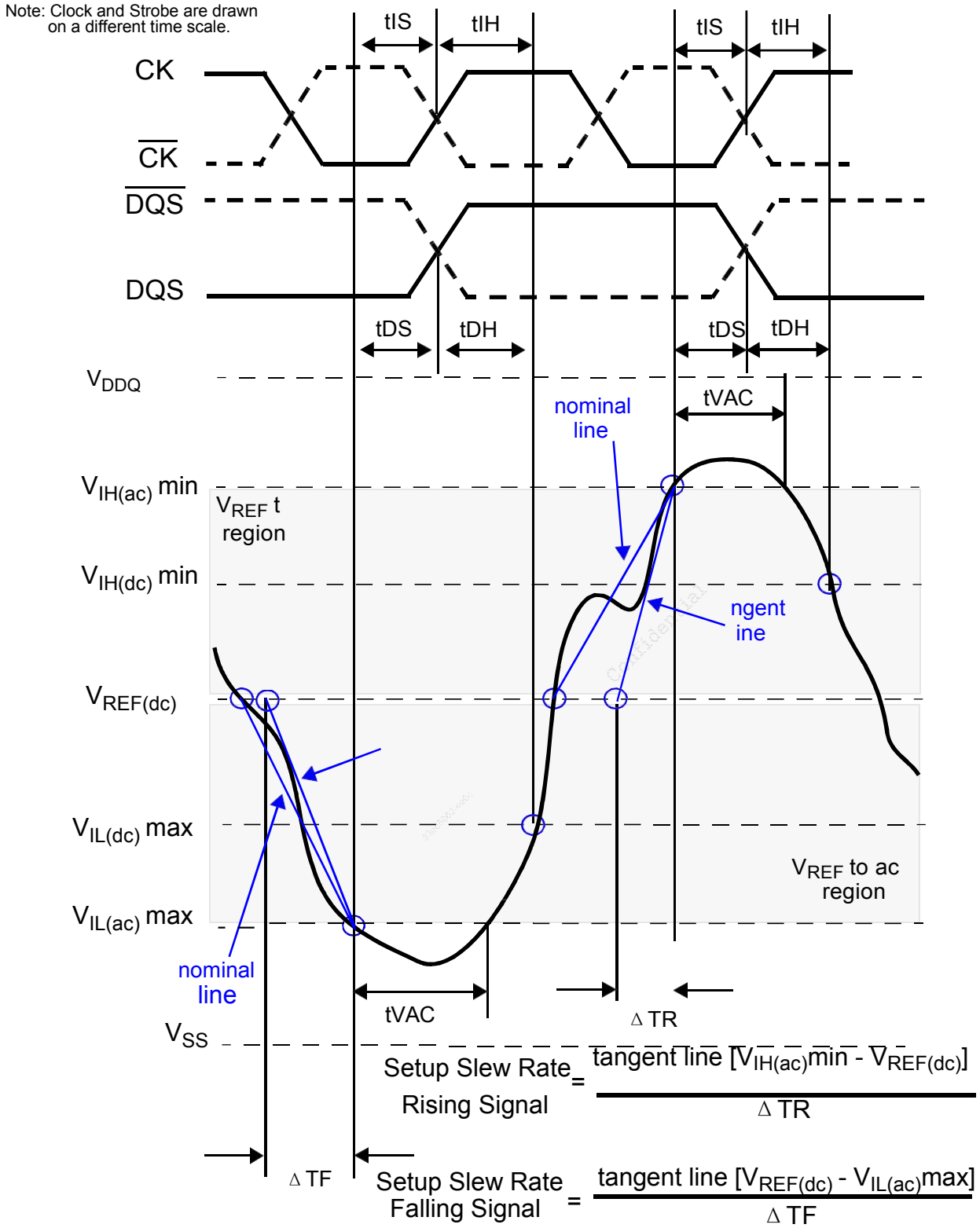
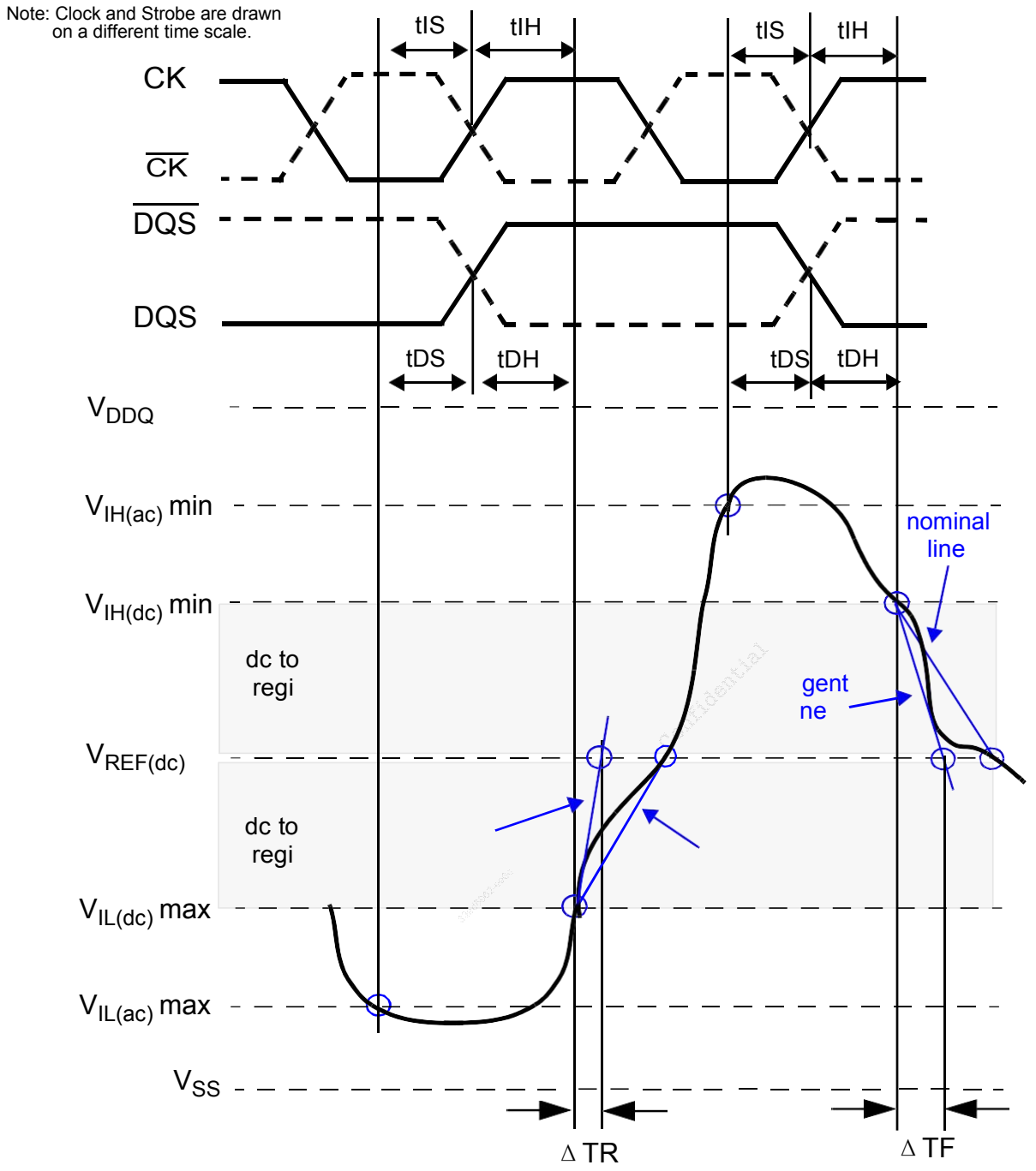


Figure 5 - Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).



$$\text{Hold Slew Rate Rising Signal} = \frac{\text{tangent line } [V_{REF(dc)} - V_{IL(dc)}\text{max}]}{\Delta\,\text{TR}}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{\text{tangent line } [V_{IH(dc)}\text{min} - V_{REF(dc)}]}{\Delta\,\text{TF}}$$

Figure 6 - Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

Data Setup, Hold and Slew Rate Derating

For all input signals the total tDS (setup time) and tDH (hold time) required is calculated by adding the data sheet tDS (base) and tDH (base) value (see Table 15) to the DtDS and DtDH (see Table 16) derating value respectively. Example: tDS (total setup time) = tDS (base) + DtDS.

Setup (tDS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IH(ac)}$min. Setup (tDS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF(dc)}$ and the first crossing of $V_{IL(ac)}$max (see Figure 7). If the actual signal is always earlier than the nominal slew rate line between shaded '$V_{REF(dc)}$ to ac region', use nominal slew rate for derating value. If the actual signal is later than the nominal slew rate line anywhere between shaded '$V_{REF(dc)}$ to ac region', the slew rate of a tangent line to the actual signal from the ac level to dc level is used for derating value (see Figure 9).

Hold (tDH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL(dc)}$max and the first crossing of $V_{REF(dc)}$. Hold (tDH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH(dc)}$min and the first crossing of $V_{REF(dc)}$ (see Figure 8). If the actual signal is always later than the nominal slew rate line between shaded 'dc level to $V_{REF(dc)}$ region', use nominal slew rate for derating value. If the actual signal is earlier than the nominal slew rate line anywhere between shaded 'dc to $V_{REF(dc)}$ region', the slew rate of a tangent line to the actual signal from the dc level to $V_{REF(dc)}$ level is used for derating value (see figure 9).

For a valid transition the input signal has to remain above/below $V_{IH/IL(ac)}$ for some time t_{VAC} (see Table 17).

Although for slow slew rates the total setup time might be negative (i.e. a valid input signal will not have reached $V_{IH/IL(ac)}$ at the time of the rising clock transition) a valid input signal is still required to complete the transition and reach $V_{IH/IL(ac)}$.

For slew rates in between the values listed in the tables the derating values may obtained by linear interpolation.

These values are typically not subject to production test. They are verified by design and characterization.

Table 15 - Data Setup and Hold Base-Values

Units [ps]	800MHz	900MHz	1.0GHz	reference
tDS (base)	10	0	TBD	$V_{IH/L(ac)}$
tDH (base)	45	45	TBD	$V_{IH/L(dc)}$

Note: (ac/dc referenced for 1V/ns DQ-slew rate and 2 V/ns DQS-slew rate)

Table 16 - Derating values tDS/tDH - ac/dc based

ΔtDS, ΔDH derating in [ps] AC/DC based [a]																	
		DQS, DQS Differential Slew Rate															
		4.0 V/ns		3.0 V/ns		2.0 V/ns		1.8 V/ns		1.6 V/ns		1.4 V/ns		1.2 V/ns		1.0 V/ns	
		ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH	ΔtDS	ΔtDH
DQ Slew rate V/ns	2.0	88	50	88	50	88	50	-	-	-	-	-	-	-	-	-	-
	1.5	59	34	59	34	59	34	67	42	-	-	-	-	-	-	-	-
	1.0	0	0	0	0	0	0	8	8	16	16	-	-	-	-	-	-
	0.9	-	-	-2	-4	-2	-4	6	4	14	12	22	20	-	-	-	-
	0.8	-	-	-	-	-6	-10	2	-2	10	6	18	14	26	24	-	-
	0.7	-	-	-	-	-	-	-3	-8	5	0	13	8	21	18	29	34
	0.6	-	-	-	-	-	-	-	-	-1	-10	7	-2	15	8	23	24
	0.5	-	-	-	-	-	-	-	-	-	-	-11	-16	-2	-6	5	10
	0.4	-	-	-	-	-	-	-	-	-	-	-	-	-30	-26	-22	-10

a.Cell contents shaded in red are defined as 'not supported'.

Table 17 - Required time t_{VAC} above VIH (ac) {below VIL (ac)} for valid transition

Slew Rate [V/ns]	t_{VAC} [ps]	
	min	max
> 2.0	75	-
2.0	57	-
1.5	50	-
1.0	38	-
0.9	34	-
0.8	29	-
0.7	22	-
0.6	13	-
0.5	0	-
< 0.5	0	-

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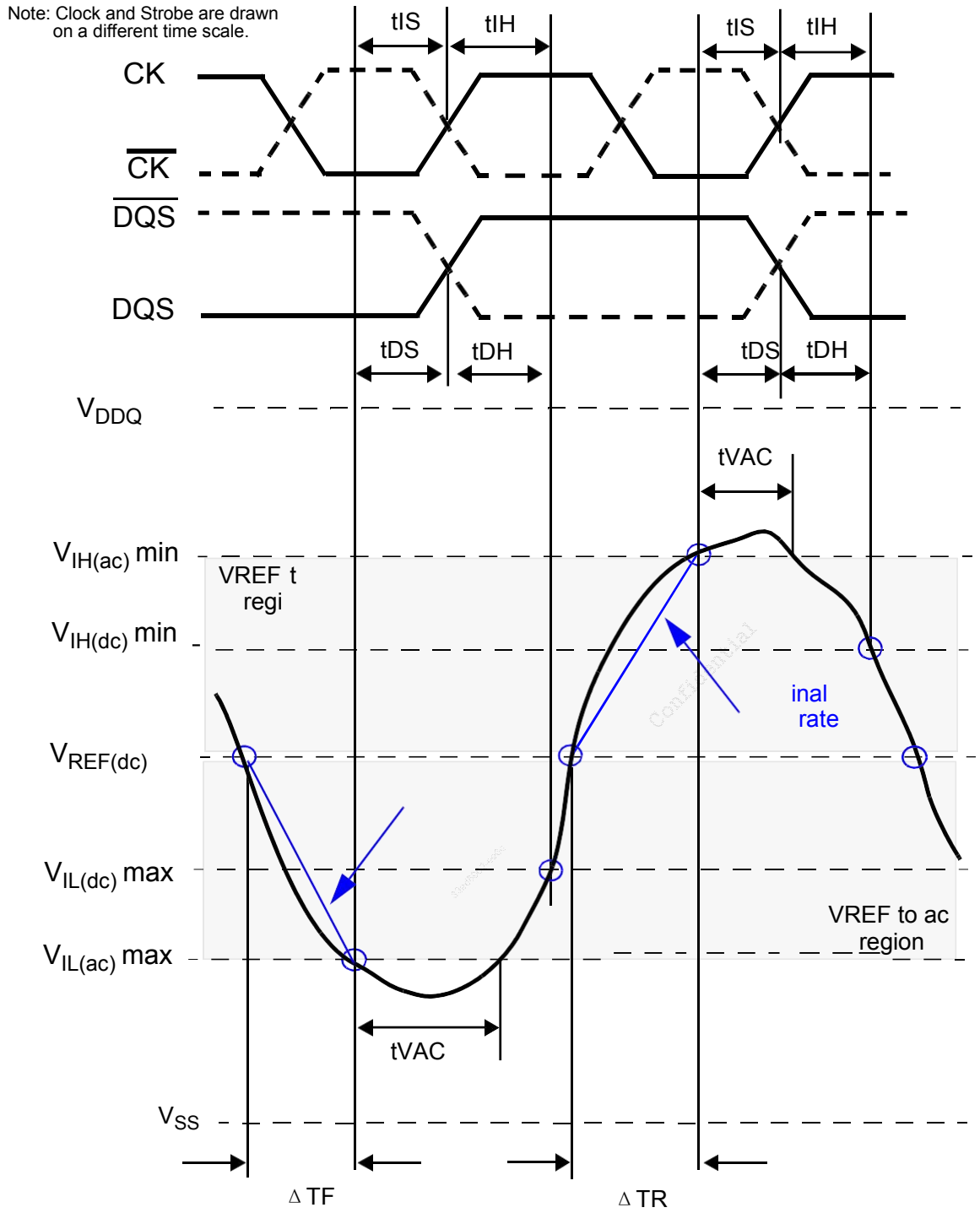

$$\text{Setup Slew Rate Falling Signal} = \frac{V_{REF(dc)} - V_{IL(ac)}max}{\Delta TF}$$

$$\text{Setup Slew Rate Rising Signal} = \frac{V_{IH(ac)}min - V_{REF(dc)}}{\Delta TR}$$

Figure 7 - Illustration of nominal slew rate and t_{VAC} for hold setup t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

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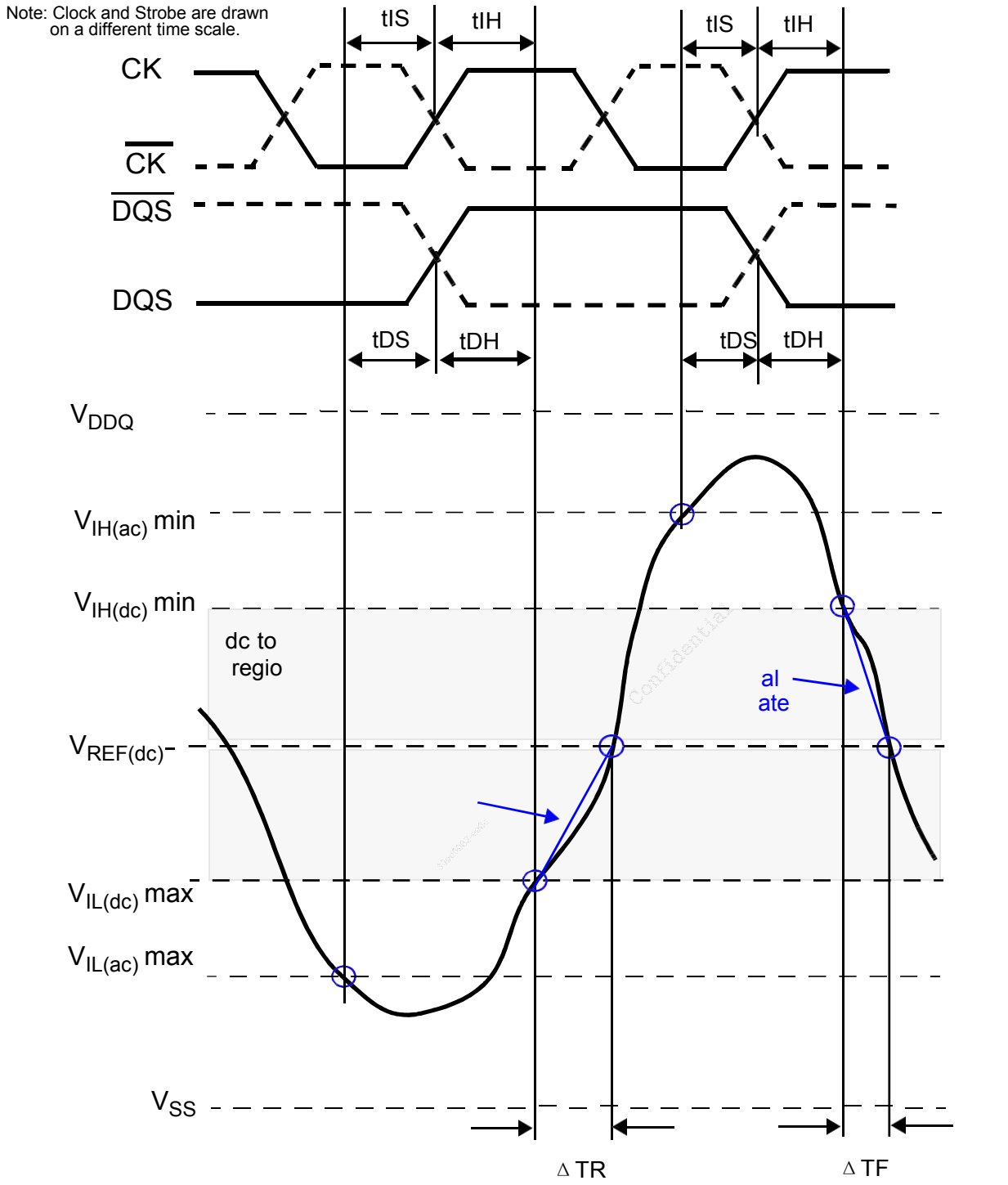

$$\text{Hold Slew Rate Rising Signal} = \frac{V_{REF(dc)} - V_{IL(dc)}max}{\Delta TR}$$

$$\text{Hold Slew Rate Falling Signal} = \frac{V_{IH(dc)}min - V_{REF(dc)}}{\Delta TF}$$

Figure 8 - Illustration of nominal slew rate for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

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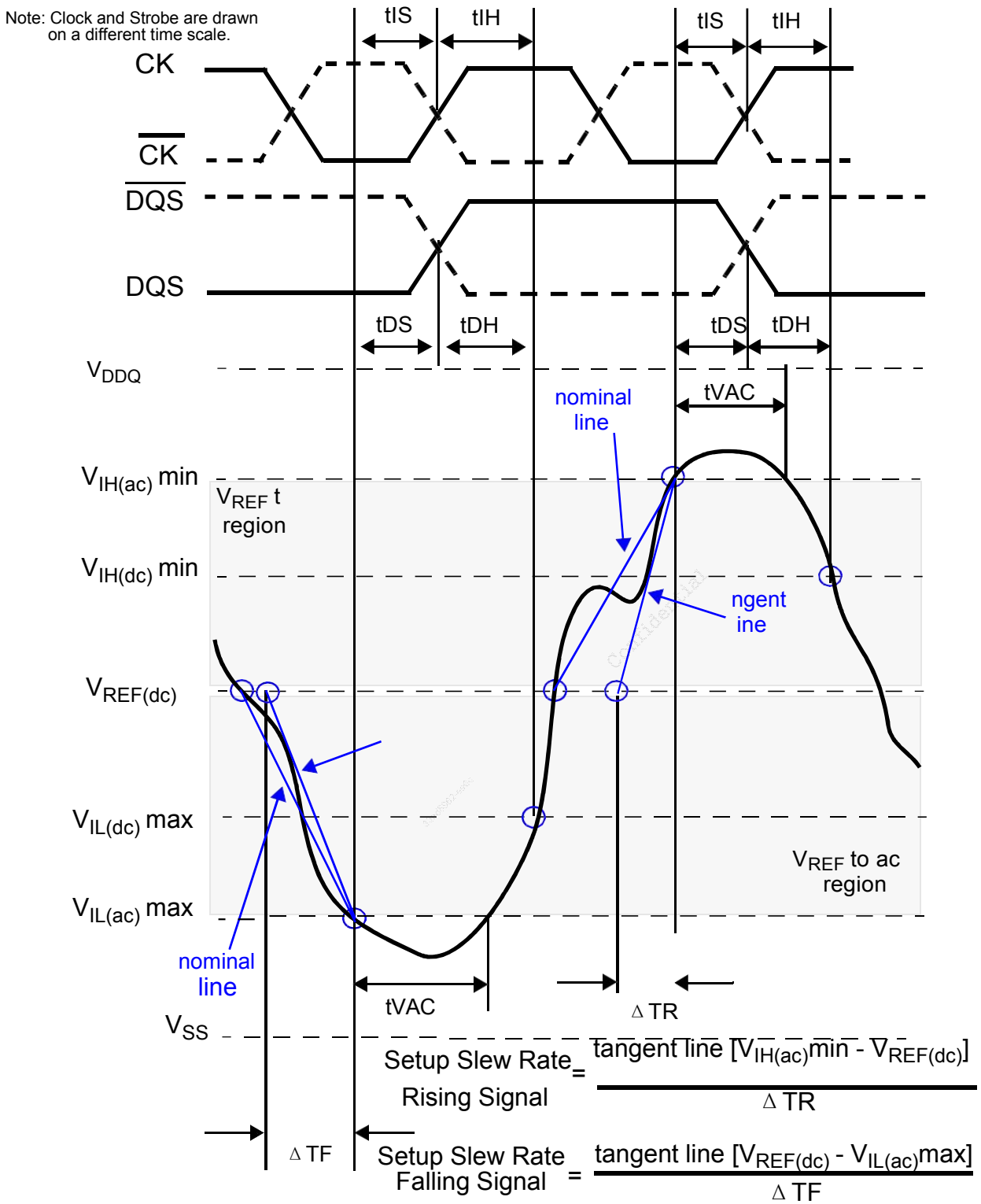


Figure 9 - Illustration of tangent line for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

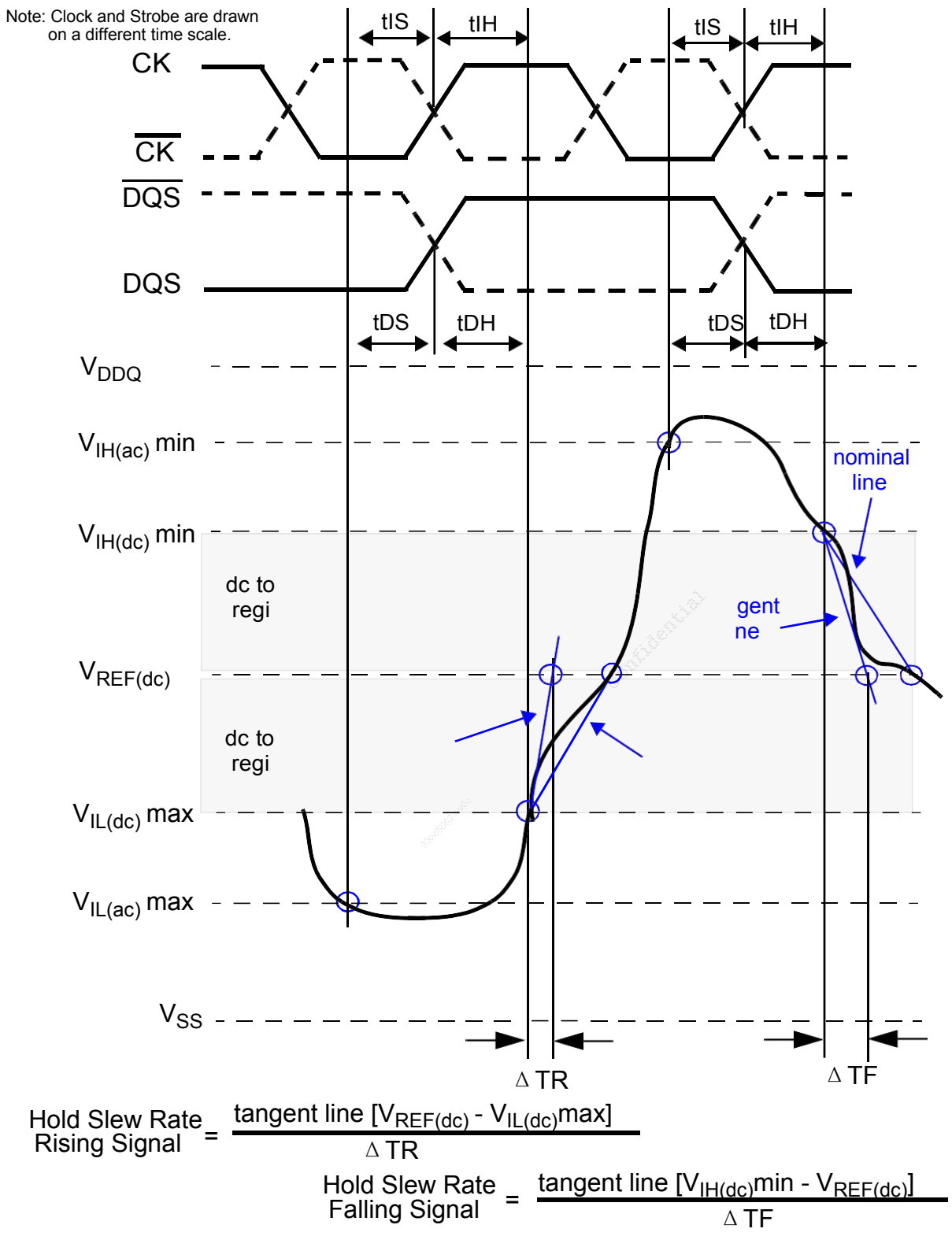
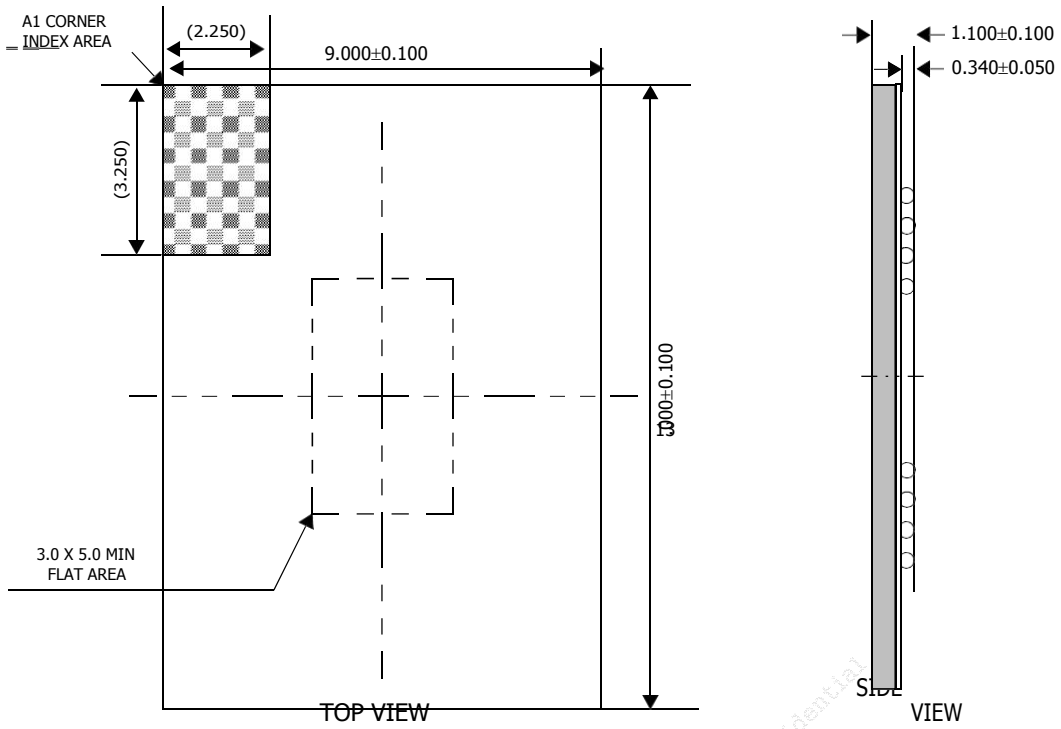
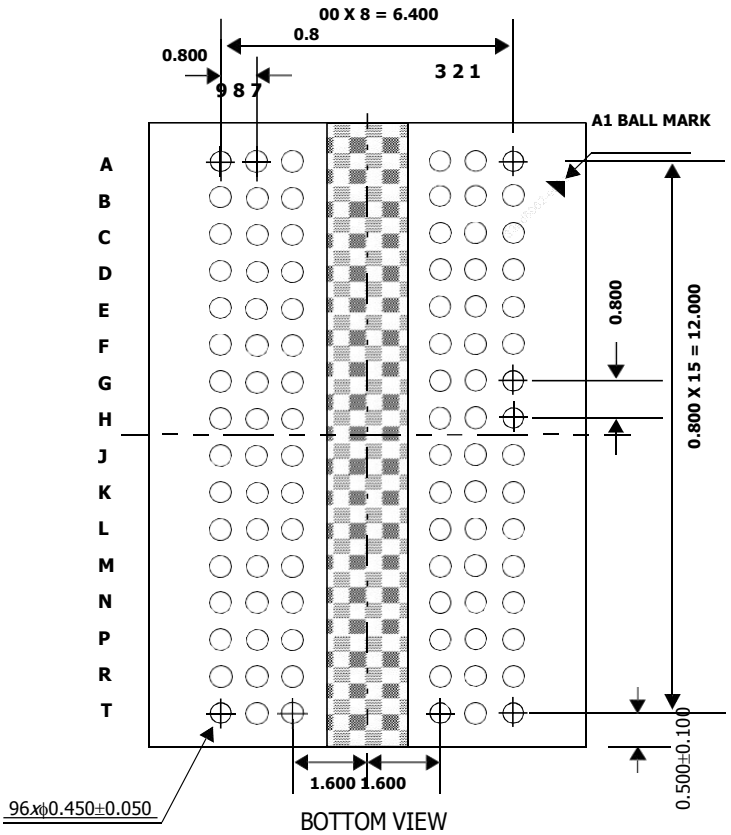


Figure 10 - Illustration of tangent line for hold time t_{DH} (for DQ with respect to strobe) and t_{IH} (for ADD/CMD with respect to clock).

12. Package Dimensions

12.1 Package Dimension(x16); 96Ball Fine Pitch Ball Grid Array Outline





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