集成 PWM 调光的串联 WLED 驱动器

特性

- 2.7V 至 5.5V 的输入电压范围
- 38V 过压保护（OVP）电压支持最多 10 颗串联 LED
- 采用创新的 CDC(Classification Drive Control)输出驱动技术，显著提升 EMI 性能
- 200mV 反馈电压
- 1% PWM 调光电流精度±20%
- 支持最低 0.3%的 PWM 调光($V_{FB.TYP}$=0.6mV)
- 1.1MHz 开关频率
- 内置过流保护和过温保护功能
- 内置软启动功能， 限制启动时的浪涌电流
- 纤小的TDFN2×2-6L 封装

概要

AW9962 是一款高效率的电感升压型白光 LED 驱动器。AW9962 内部集成了 40V 的功率开关， 可支持单串最多 10 颗 LED 应用。AW9962 的 1.1MHz 固定工作频率减小了输出电压纹波， 提高了转换效率，而且允许使用封装更小的外围器件。

AW9962 的反馈电压为 200mV，如典型应用图所示， LED 的电流通过外置设定电阻确定。AW9962 支持 PWM 调光方式， LED 的电流可通过加在 CTRL 引脚的 PWM 调光信号的占空比来控制。

AW9962 内置软启动功能，最大限度地减小电源的浪涌电流。 AW9962 还内置过流保护、LED 开路过压保护（OVP）及过温保护， 防止芯片进入异常工作状态。

应用

移动电话

便携式多媒体播放器

PDAs

- GPS 接收器
-
-
-

典型应用图

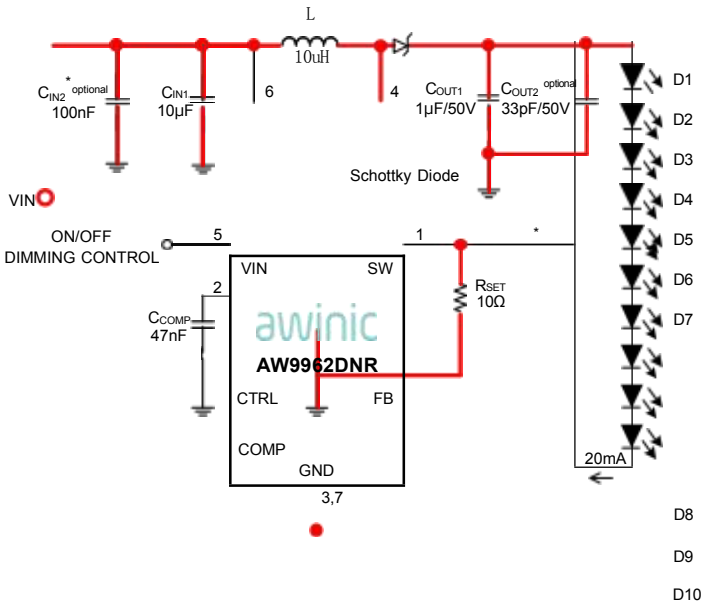
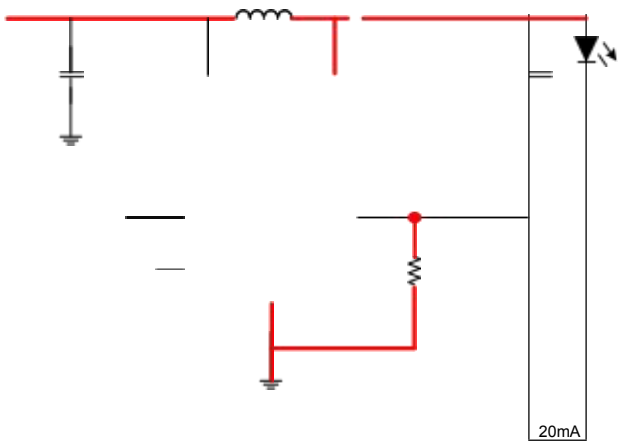


图 1　AW9962 典型应用图



White LED Driver with PWM Brightness Control in Small Package

FEATURES

- 2.7V to 5.5V Input Voltage Range
- 38V Over-voltage Protection for up to 10 LEDs in Series
- Innovative CDC Output Drive Technology, Significantly Improve EMI Performance
- 200mV Reference Voltage
- 1% PWM dimming current accuracy ±20%
- Support 0.3% PWM dimming($V_{FB.TYP}$=0.6mV)
- 1.1MHz Switching Frequency
- Over-current and Over-temperature Protection
- Built-in Soft-start Limits Inrush Current
- Ultra Small 2mm*2mm TDFN-6L package

APPLICATIONS

- Mobile Phones
- Portable Media Players
- PDAs
- GPS Receivers

GENERAL DESCRIPTION

The AW9962 is a white LED driver with integrated boost converter. With an internal 40V switch FET, the AW9962 drives up a string of up to 10 LEDs in series. The boost converter runs at 1.1MHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components.

The default white LED current is set with the external sense resistor R_{SET}, and the feedback voltage is regulated to 200mV, as shown in the typical application. During the operation, a pulse width modulation (PWM) signal can be applied to the CTRL pin through which the duty cycle determines the feedback reference voltage.

AW9962 integrates built-in soft-start function to minimize the power supply inrush current. AW9962 also integrates over-current protection , LED open protection and over temperature protection(OTP) to prevent chip from entering abnormal operating conditions.

TYPICAL APPLICATION CIRCUIT

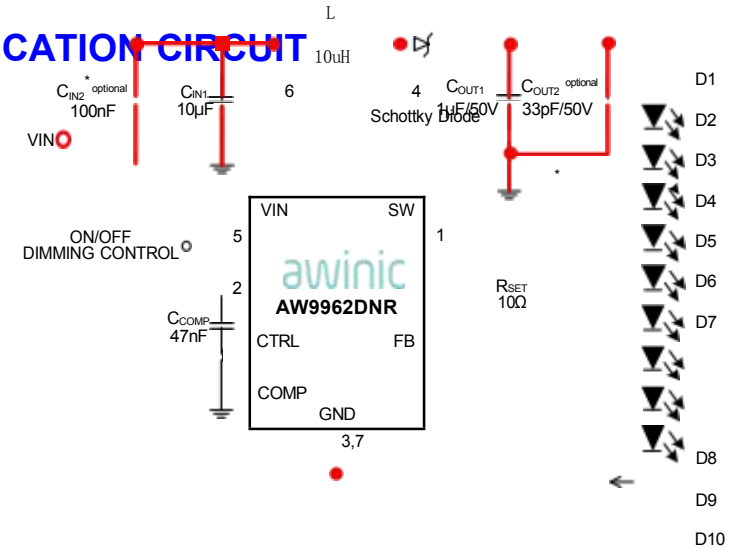
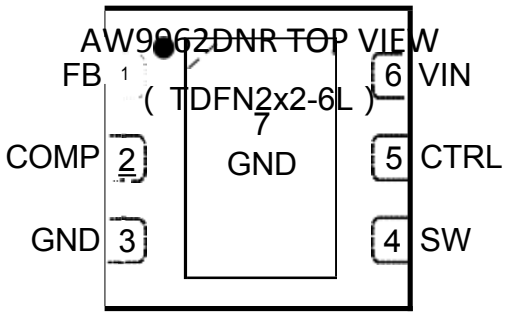
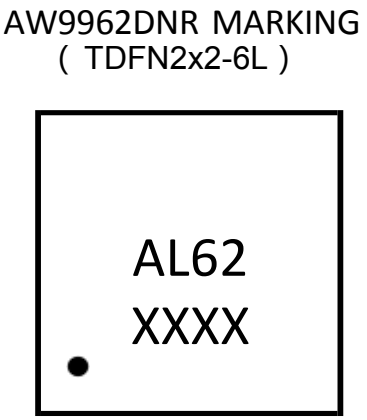


Figure 1 Typical Application Circuit of AW9962

PIN CONFIGURATION AND TOP MARK





Top Mark

AL62—AW9962DNR

XXXX—Manufacture Data

Figure 2 Pin Configuration and NAME

PIN DEFINITION

No.		DESCRIPTION
1	FB	Feedback pin for current. Connect the sense resistor from FB to GND.
2	COMP	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the regulator.
3	GND	Ground.
4	SW	This is the switching node of the IC. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection.
5	CTRL	Control pin of the boost regulator. It is a pin which can be used for PWM digital dimming.
6	VIN	The input supply pin for the IC. Connect VIN to a supply voltage between 2.7V and 5.5V.
7	GND	Exposed pad should be soldered to PCB board and Connected to GND.

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FUNCTIONAL BLOCK DIAGRAM

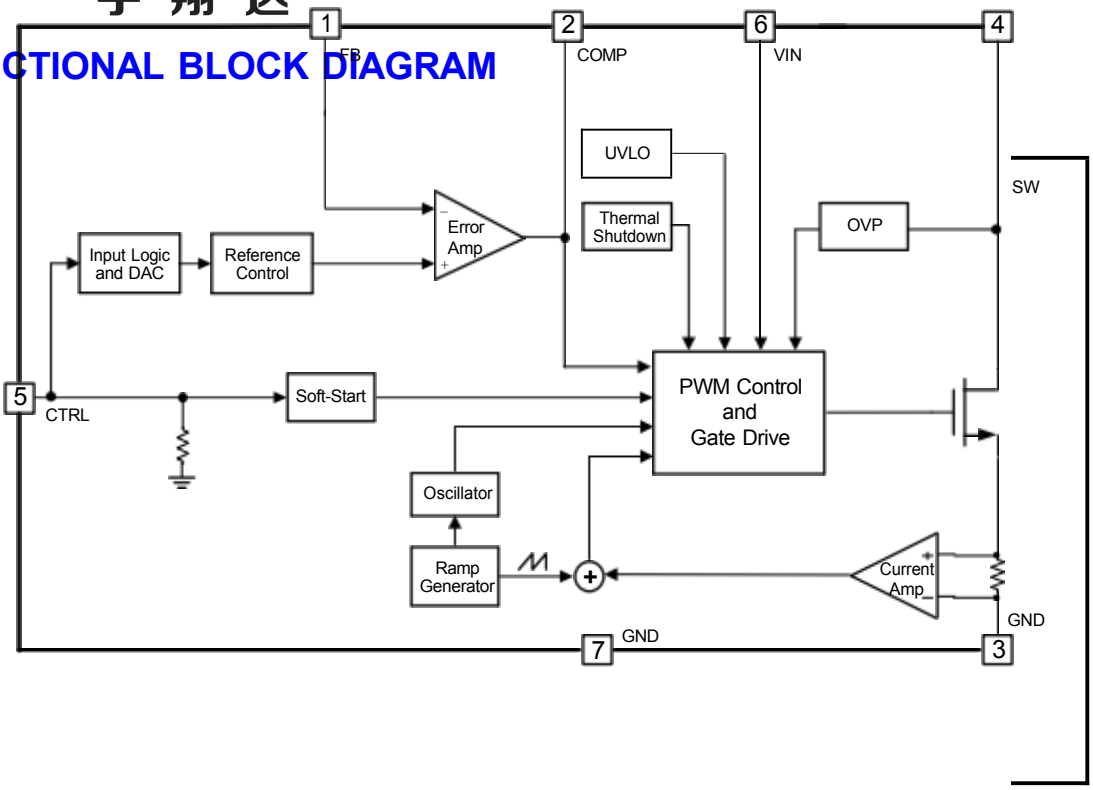


Figure 3 FUNCTIONAL BLOCK DIAGRAM

TYPICAL APPLICATION CIRCUITS

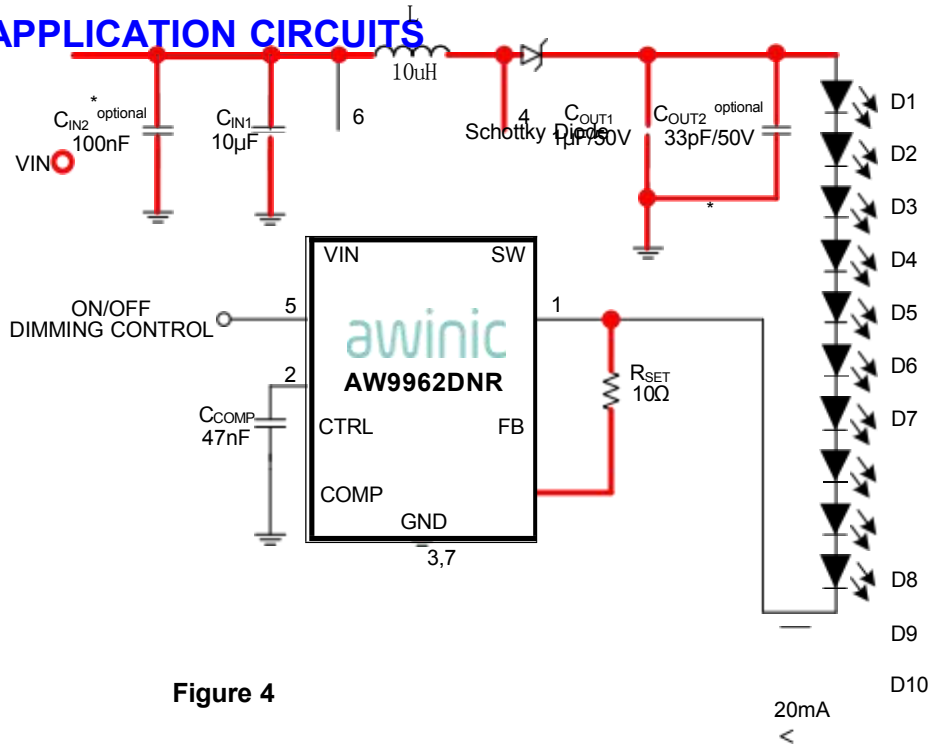
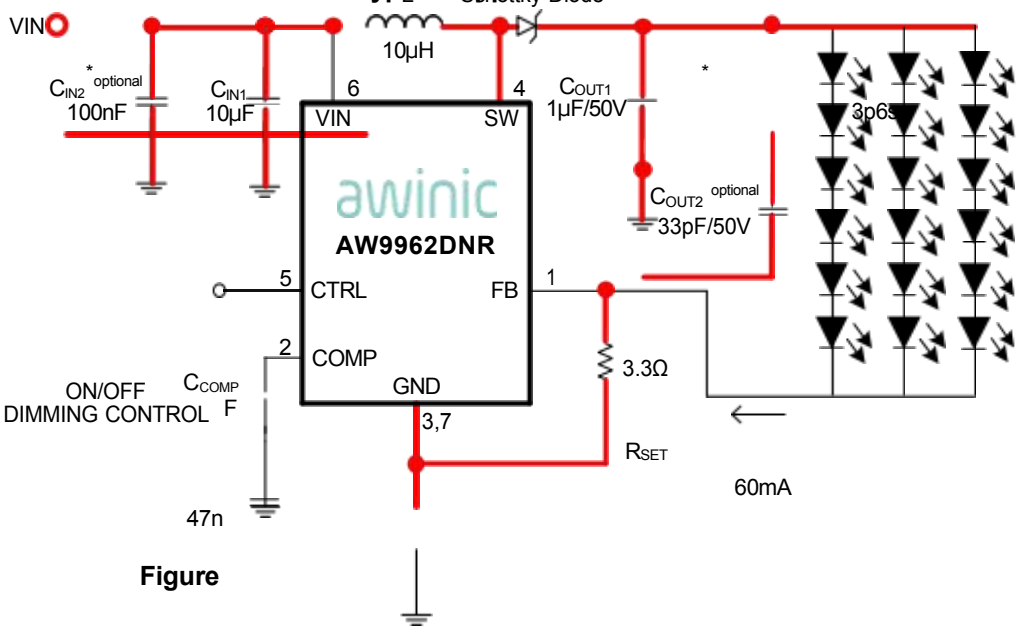


Figure 4

Typical Application of AW9962



Figure

5 Drive 18 White LEDs for Big Screen Display

Notice for Typical Application Circuits:

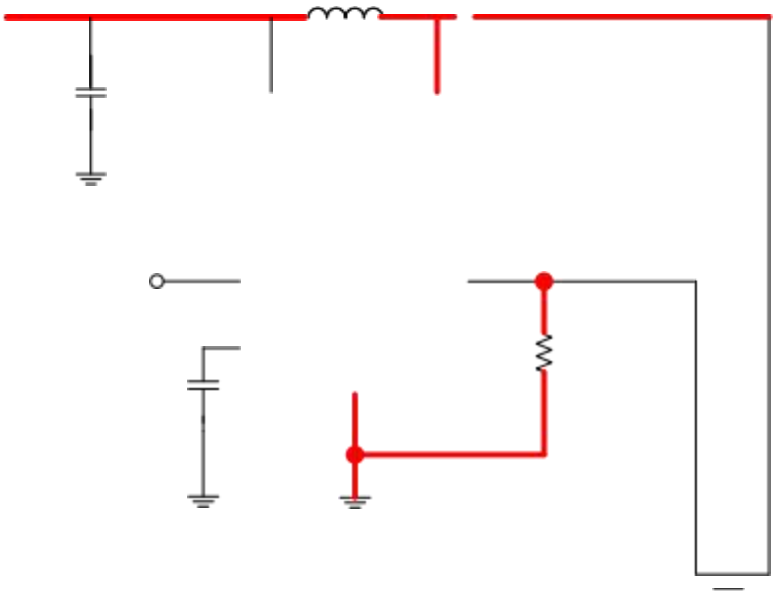
1：Recommended device for AW9962:

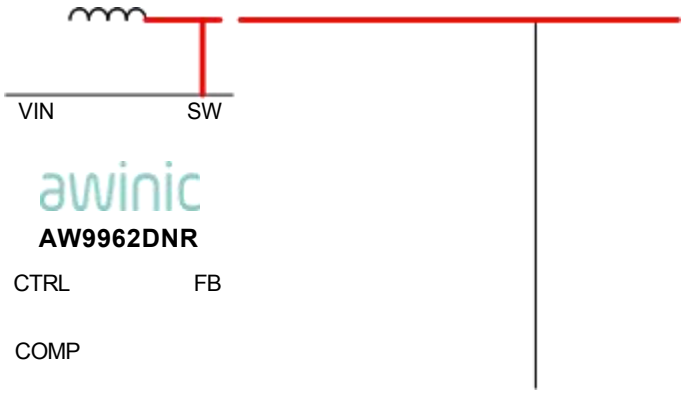
L: LQH3NPN100NM0

C_{IN1}: Murata GRM188R61C106MA73

C_{IN2}: Murata GRM155R61C104K

C_{OUT1}: Murata GRM21BR71H105KA





C_{OUT2}: Murata GRM1555C1H330GA

Schottky Diode: ONsemi MBR0540T1

2：C_{IN2} and C_{OUT2} are recommended to use in parallel with the input capacitor and output capacitor to suppress high frequency noise.

3：Red lines are high current paths, reference to the section APPLICATION INFORMATION.

4：The capacitors (C_{IN1}, C_{IN2}, C_{OUT1}, C_{OUT2} and C_{COMP}) should be placed as close to the pins of the IC as possible.

5：Minimize trace lengths between the IC and the inductor, the Schottky diode and the output capacitor, keep these traces short, direct, and wide.

6：Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	Delivery Form
AW9962DNR	-40℃～85℃	TDFN2x2-6L	AL62	3000 units/ Tape and Reel

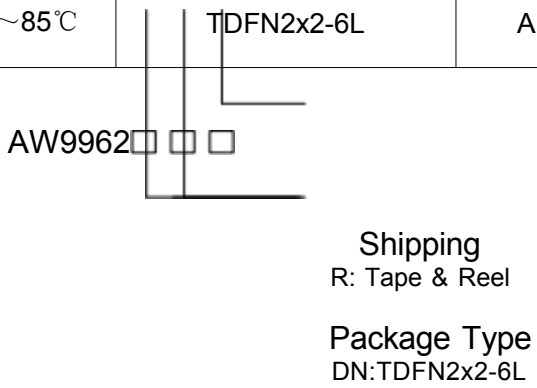


Figure 6 Package Information

ABSOLUTE MAXIMUM RATINGS(NOTE1)

PARAMETERS	RANGE
Supply voltage range VIN(NOTE 2)	-0.3V to 6V
Voltage on FB,CTRL and COMP(NOTE 2)	-0.3V to 6V
Voltage on SW(NOTE 2)	-0.3V to 40V
Junction-to-ambient thermal resistance θ_{JA}	65℃/W
Operating free-air temperature range	-40℃ to 85℃
Maximum Junction temperature T_{JMAX}	160℃
Storage temperature T_{STG}	-65℃ to 150℃
Lead Temperature (Soldering 10 Seconds)	260℃
ESD(NOTE 3)	
ALL PINS HBM (human body model) (NOTE 4)	±6000V
ALL PINS CDM (charge device model) (NOTE 5)	±2500V
ALL PINS MM (machine model) (NOTE 6)	±300V
Latch-up(NOTE 7)	
Latch-up current maximum rating per JEDEC standard	+IT：250mA -IT：-250mA

NOTE1: Conditions out ofthose ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite ofthe limits above, functional operation conditions ofthe device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: All voltage values are with respect to network ground terminal.

NOTE3: This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. AWINIC recommends that all integrated circuits b handled with appropriate precautions. Failure to observe proper

handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

NOTE4: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883H Method 3015.8.

NOTE5: Test Condition: JEDEC EIA/JESD22-C101E.

NOTE6: Test Condition: JEDEC EIA/JESD22-A115.

NOTE7: Test Condition: JEDEC STANDARD NO.78D NOVEMBER 2011.

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ELECTRICAL CHARACTERISTICS

Test Condition: T_A = 25℃, VIN = 3.6V, V_{CTRL} = VIN (Unless otherwise specified).

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT						
VIN	Input voltage range		2.7		5.5	V
I_Q	Operating quiescent current	VFB = 1V		1.6		mA
I_{SD}	Shutdown current	V_{CTRL} = GND, VIN=4.2V		0.1	1	μA
UVLO	Under-voltage lockout threshold	VIN falling		2.2	2.39	V
V_{hys}	Under-voltage lockout hysteresis			100		mV
ENABLE AND REFERENCE CONTROL						
$V_{(CTRLh)}$	CTRL logic high voltage	VIN = 2.7V to 5.5V	1.5			V
$V_{(CTRLl)}$	CTRL logic low voltage	VIN = 2.7V to 5.5V			0.3	V
$R_{(CTRL)}$	CTRL pull down resistor			600		kΩ
t_{off}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		197	200	203	mV
$V_{(REF\_PWM)}$	Voltage feedback regulation voltage under brightness control	f_{PWM} = 20 kHz, duty cycle = 1%	1.6	2	2.4	mV
		f_{PWM} = 20 kHz, duty cycle = 0.3%		0.6		mV
I_{FB}	Voltage feedback input bias current			0.1	1	μA
f_S	Oscillator frequency			1100		KHz
D_{max}	Maximum duty cycle		90%	95%		
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	VIN = 3.6V		0.36	0.65	Ω
		VIN = 3.0V			0.7	Ω
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35V, T_A = 25℃			1	μA

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
OCP AND OVP						
I_{LIM}	N-channel MOSFET current limit			2		A

V_{OVP}	Open LED overvoltage protection threshold	Measured on the SW pin		38		V

t_{REF}	VREF filter time constant			480		μs
PWM DIMMING TIMING						
f_{PWM}	Frequency of PWM dimming		10		100	kHz
t_{min_on}	Minimum on pulse width			50		ns
THERMAL SHUTDOWN						
T_{OTP}	Thermal shutdown threshold			165		℃
T_{hys}	Thermal shutdown threshold hysteresis			16		℃

TYPICAL CHARACTERISTICS

Table 1 TABLE OF FIGURES

INDEX		FIGURE No.
Efficiency 1	VIN=3.6V; 4,6,8,10 LEDs; L=10μH	FIGURE 7
Efficiency 2	VIN=4.2/3.6/3.0V; 10 LEDs, L=10μH	FIGURE 8
Efficiency 3	VIN=2.5~5.5V; 1P10S, 2P8S,3P8S LEDs, L=10μH	FIGURE 9
Switching frequency	VIN=2.5~5.5V, 10 LEDs, L=10μH	FIGURE 10
PWM dimming linearity	PWM Freq = 20 kHz	FIGURE 11
Feedback voltage line regulation	VIN=2.5~5.5V	FIGURE 12
Soft-start waveform	VIN=3.8V, 10 LEDs, L=10μH	FIGURE 13
Switching waveform	VIN=3.8V, 10 LEDs, L=10μH	FIGURE 14
Open LED protection	VIN=3.6V, 10 LEDs, L=10μH	FIGURE 15

EFFICIENCY Vs. OUTPUT CURRENT

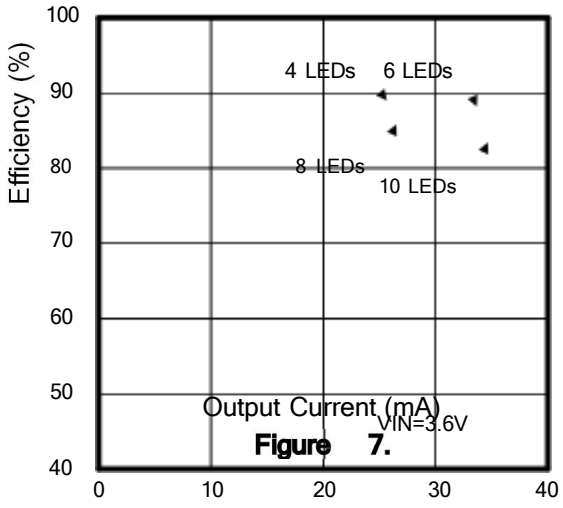


Figure 7.

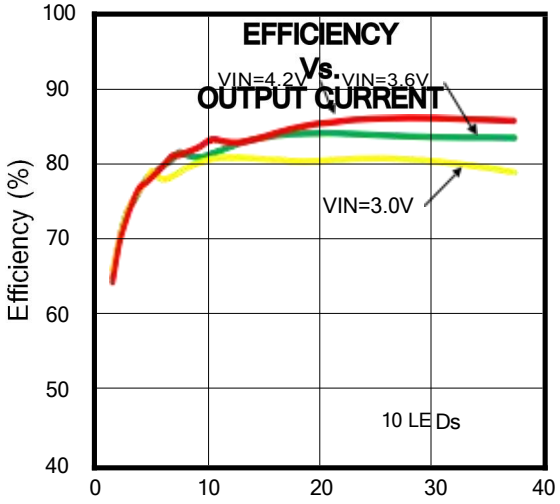


Figure 8.

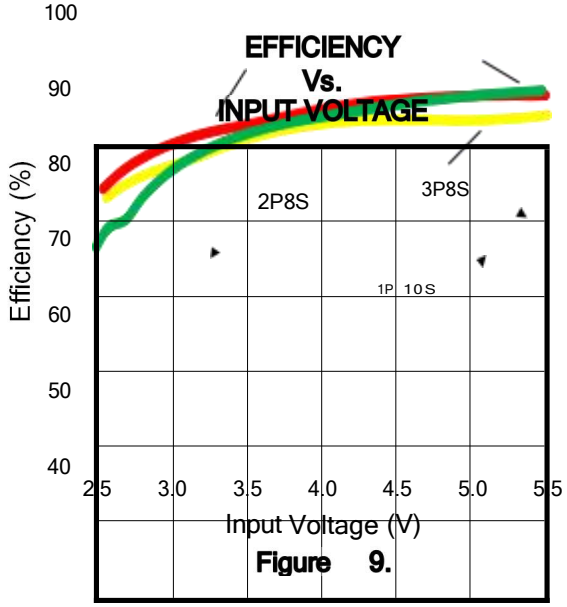


Figure 9.

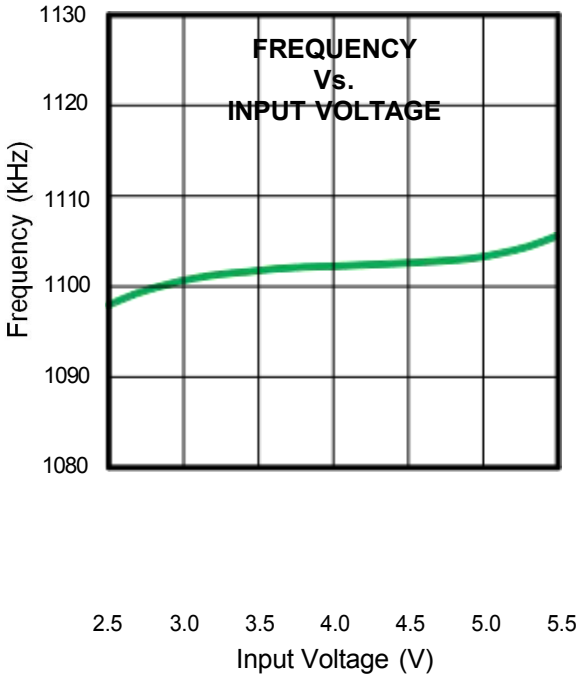


Figure 10.

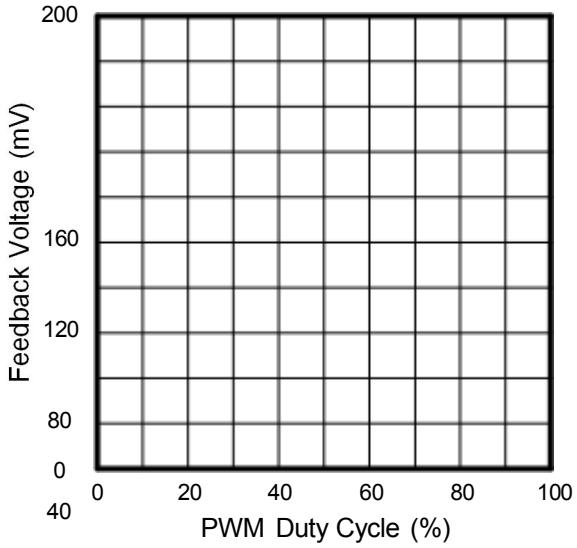


Figure 11.

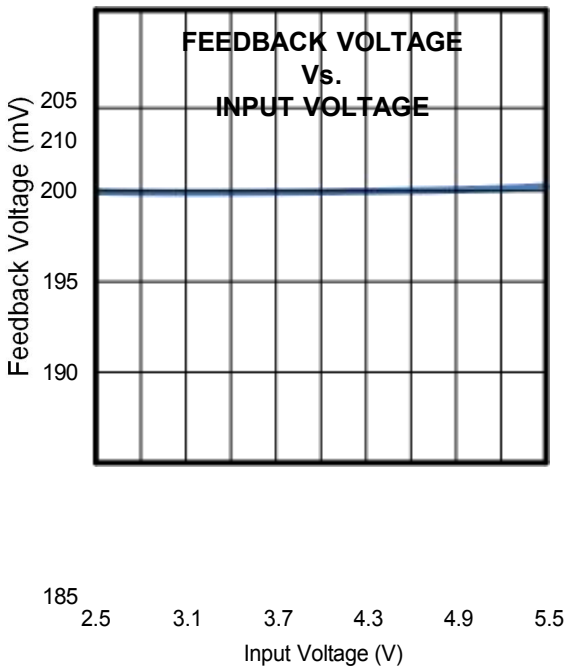


Figure 12.

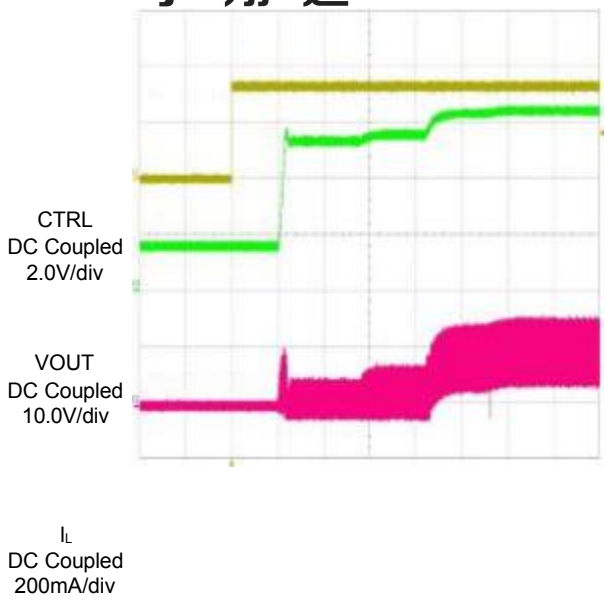


Figure 13.

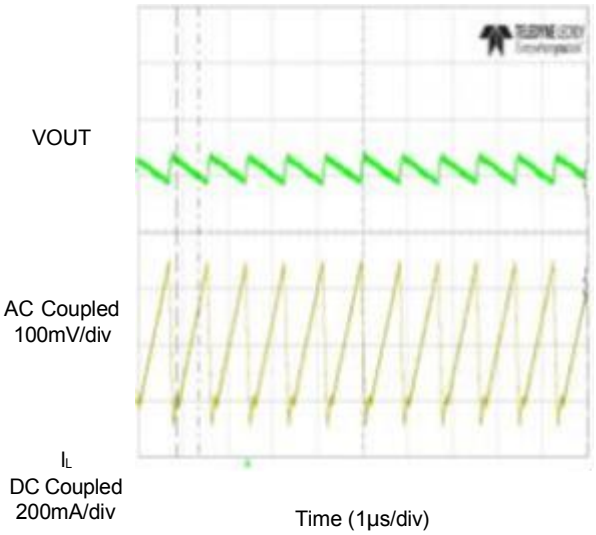


Figure 14.

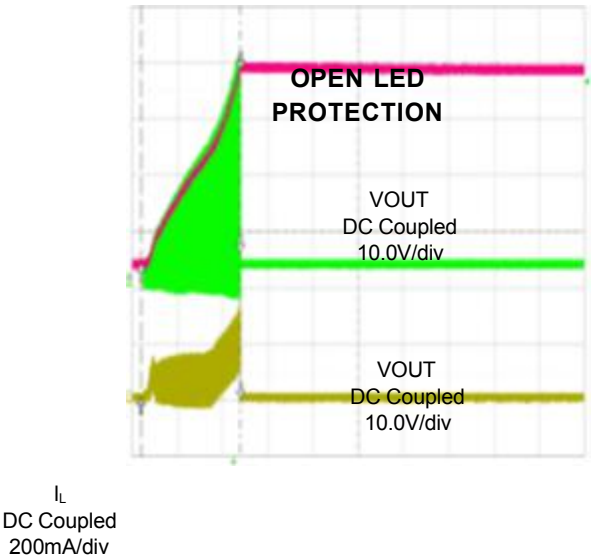


Figure 15.

DETAILED FUNCTIONAL DESCRIPTION

The AW9962 is a high efficiency, high output voltage boost converter in small package size. The device is ideal for driving up to 10 white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs. The device integrates 40V/2.0A switch FET and operates in pulse width modulation (PWM) with 1.1MHz fixed switching frequency. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control. Therefore, slope compensation is added to the current signal to allow stable operation for duty cycle larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200mV typical), reducing the power dissipation in the current sense resistor.

START-UP

SOFT

LED OVER-VOLTAGE PROTECTION

Soft-start circuitry is integrated into the IC to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage. This ensures that the output voltage rises slowly to reduce the input current.

OPEN

Open LED over-voltage protection circuitry prevents IC damage as the result of white LED disconnection. The AW9962 monitors the voltage at the SW pin during each switching cycle. The circuitry turns off the switch FET as soon as the SW voltage exceeds the V_{OVP} threshold for 8 clock cycles.

SHUTDOWN

The CTRL input is used to enable or disable the AW9962. Pulling the CTRL pin higher than 1.5V will enable the device. The AW9962 has an internal shutdown delay circuitry, when the CTRL pin is held low for an amount of time longer than 2.5ms, the AW9962 will enter shutdown mode and the input supply current for the device is less than 1μA. Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

LOCKOUT

UNDER-VOLTAGE

PROGRAM

An under-voltage lockout prevents operation of the device at input voltage below typical 2.2V. When the input voltage is below the under-voltage threshold, the internal switch FET is turned off. If the input voltage rises by under-voltage lockout hysteresis, the IC restarts.

CURRENT

The FB voltage is regulated by a low 200mV reference voltage. The LED current is programmed externally using a current sense resistor in series with the LED string. The value of the R_{SET} can be calculated by the following equation:

$$R_{SET} = \frac{V_{FB}}{I_{LED}} \quad (1)$$

Where:

I_{LED} = output current of LEDs

V_{FB} = regulated voltage of FB

R_{SET} = current sense resistor

PWM BRIGHTNESS DIMMING

When the CTRL pin is constantly high, the FB voltage is regulated to 200mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage, it achieves LED brightness dimming. The relationship between the duty cycle and the FB voltage is given by the following equation:

$$V_{FB} = \text{Duty} \times 200mV \qquad (2)$$

Where:

Duty = duty ~~cycle of the~~ PWM signal

200mV = internal reference voltage

As shown in the FIGURE 16, the IC chops up the internal 200mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, AW9662 regulation voltage is independent of the PWM logic voltage level which often has large variations.

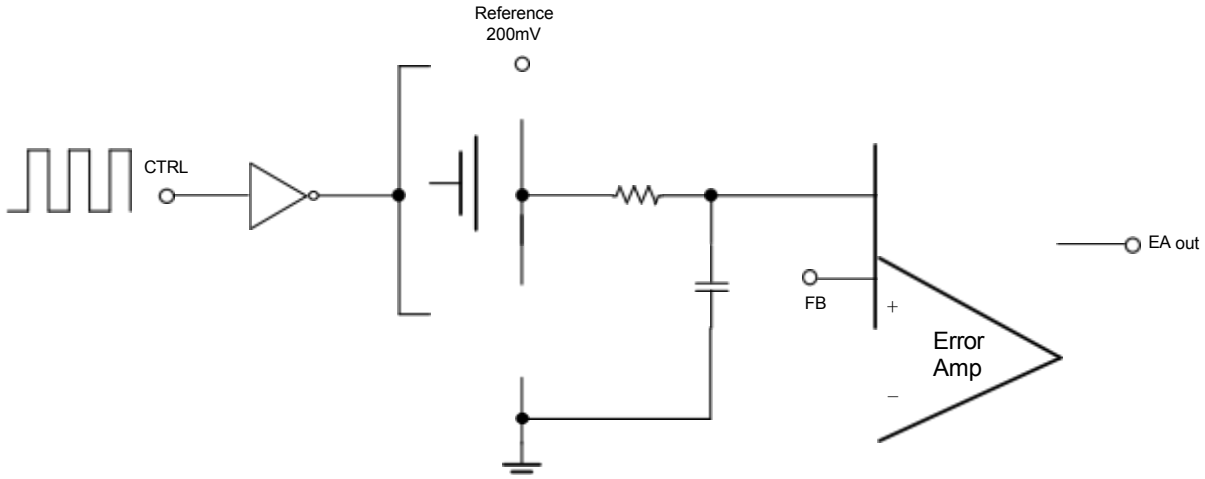


Figure16 Block Diagram of Programmable FB Voltage Using PWM Signal

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of is exceeded 165℃. The device is released from shutdown automatically when the junction temperature decreases by 16℃.

APPLICATION INFORMATION

MAXIMUM OUTPUT CURRENT

The over-current limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. The current limit setting, input voltage, output voltage and efficiency can all change maximum current output. Therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. The following equations take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{V_{OUT} + V_F - VIN}{[L \times F_s \times (\frac{1}{VIN} + \frac{1}{V_{OUT} + V_F - VIN})]} \quad (3)$$

Where:

I_P = inductor peak to peak ripple

L= inductor value

V_F = Schottky diode forward voltage

F_S = switching frequency

V_{OUT} = output voltage of the boost converter. It is equal to the sum of V_{FB} and the voltage drop across LEDs.

$$I_{out\_max} = \frac{VIN \times (I_{lim} - I_P / 2) \times \eta}{V_{OUT}} \quad (4)$$

Where:

I_{out_max} = maximum output current of the boost converter

I_{lim} = over-current limit, for worst case calculation the minimum value has to be chosen.

η = efficiency

INDUCTOR

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating. The inductor DC current is given by:

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{out}}{VIN \times \eta} \quad (5)$$

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor

SELECTION

vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value provides much more output current and higher conversion efficiency. For these reasons, a

4.7μH to 10μH inductor value range is recommended. A 10μH inductor optimized the efficiency for most application while maintaining low inductor peak to peak ripple.TABLE 2lists the recommended inductor for the AW9962. When recommending inductor value, the factory has considered –40% and +20% tolerance from its nominal value.

Table 2 Recommended Inductors for AW9962

Part Number	L (μH)	DCR Max (Ω)	Saturation Current (mA)	Size (L x W x H mm)	Vendor
LQH3NPN100NM0	10	0.3	750	3 x 3 x 1.5	Murata
A997AS-220M	22	0.4	510	4 x 4 x 1.8	TOKO
CDH3809/SLD	10	0.3	570	4 x 4 x 1.0	Sumida
LPS4018-472ML	4.7	0.125	1900	4 x 4 x 1.8	Coilcraft

DIODE SELECTION

The high switching frequency of the AW9962 demands a high-speed rectification for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED over-voltage protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for AW9962.

SCHOTTKY

CAPACITOR SELECTION

COMPENSATION

The compensation capacitor C_{COMP} (see the application circuit), connected from COMP pin to GND, is used to stabilize the feedback loop of the AW9962. Use 47nF X5R or X7R ceramic capacitor for C_{COMP}.

For most applications, ceramic capacitors with X7R or X5R temperature characteristic are preferred for use with the AW9962.

Capacitors with Y5V or Z5U temperature characteristic are generally not recommended for use with the AW9962.

CAPACITORS SELECTION

INPUT AND OUTPUT

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - VIN) \times I_{out}}{V_{OUT} \times F_S \times V_{ripple}} \quad (6)$$

Where, V_{ripple} = peak-to-peak output ripple. The additional output ripple component caused by ESR is calculated using:

$$V_{ripple\_ESR} = I_{out} \times R_{ESR} \quad (7)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequency in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce

capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

An X5R or X7R capacitor of 10μF is recommended for input side. The output requires a X5R or X7R capacitor in the range of 0.47μF to 4.7μF. A 100nF capacitor and a 33 pF capacitor are recommended to use in parallel with the input capacitor and the output capacitor to suppress high frequency noise.

The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. For example, if use the output capacitor of 0.1μF, a 470nF compensation capacitor has to be used for the loop stable.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

POWER DISSIPATION

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the AW9962. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined by using the following equation:

Where, T_{Jmax}

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{\theta_{ja}}$$

The AW9962 is the Maximum Junction Temperature, T_A is the maximum ambient temperature for the application. θ_{ja} is the thermal resistance junction-to-ambient given in Power Dissipation Table.

comes in a thermally enhanced TDFN package. Compared with the TSOT package, the TDFN package has better heat dissipation. This package includes a thermal pad that improves the thermal capabilities of the package. The θ_{ja} of the TDFN package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered directly to the analog ground on the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit(IC).

Using thermal vias underneath the thermal pad as illustrated in the layout example.

PCB LAYOUT CONSIDERATION

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and should be kept as short as possible.

The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce the IC supply ripple.

Connect the exposed paddle to the PCB ground plane using at least two vias. The input and the output bypass capacitors should be placed as close to the IC as possible. Minimize trace lengths between the IC and the inductor, the diode and the output capacitor; keep these traces short, direct, and wide.

A recommended PCB Layout is shown in FIGURE 17. In order to dissipate the package heat, the package thermal pad must be connected to a large copper area on the ground plane underneath using multiple vias.

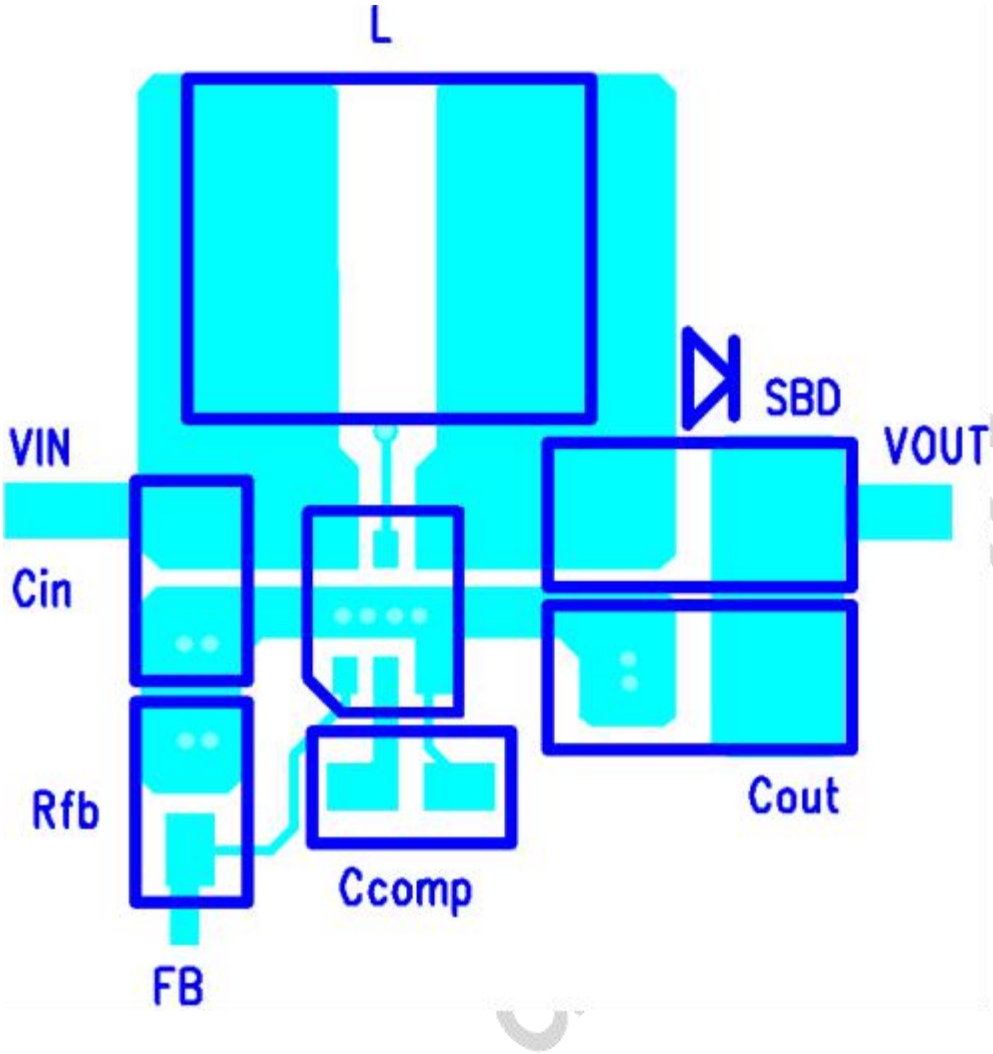
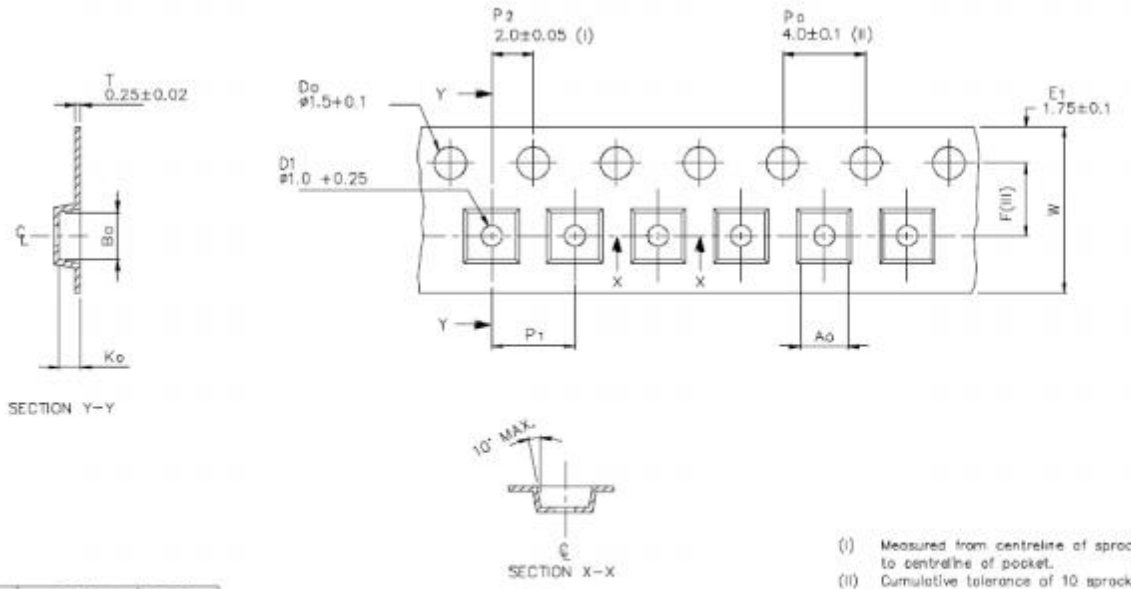


Figure 17 Recommended PCB Layout

TAPE AND REEL INFORMATION

Carrier Tape

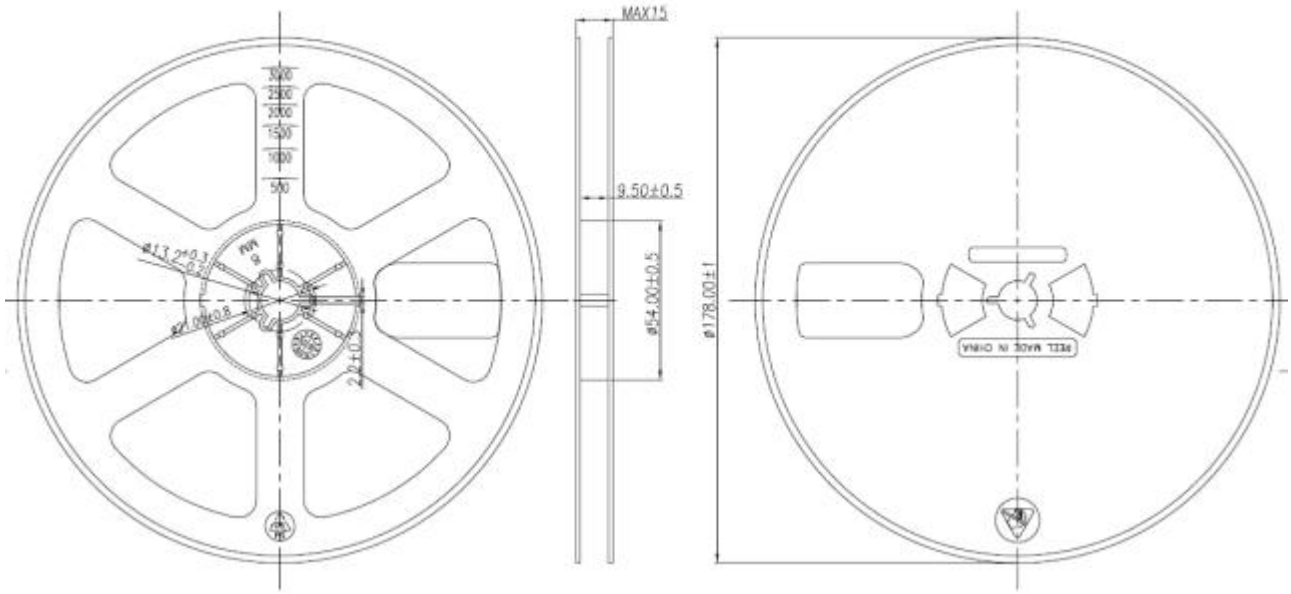


Ao	2.30 +/−0.05
Bo	2.30 +/−0.05
Ko	1.00 +/−0.05
F	3.50 +/−0.05
P1	4.00 +/−0.1
W	8.00 +0.3/−0.1

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.
(V) Typical SR of form tape Max 10^9 OHM/SQ

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Reel



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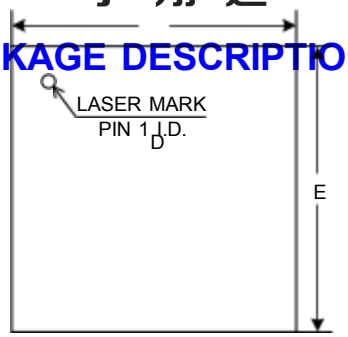
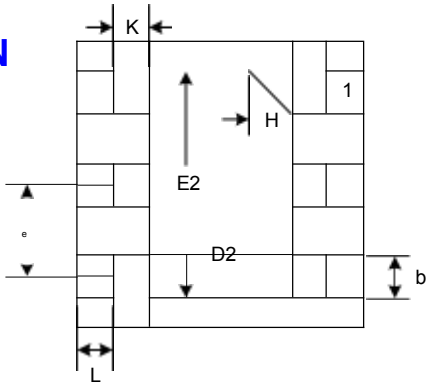
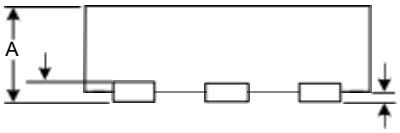
PACKAGE DESCRIPTION



TOP VIEW



BOTTOM VIEW



SIDE VIEW

A1

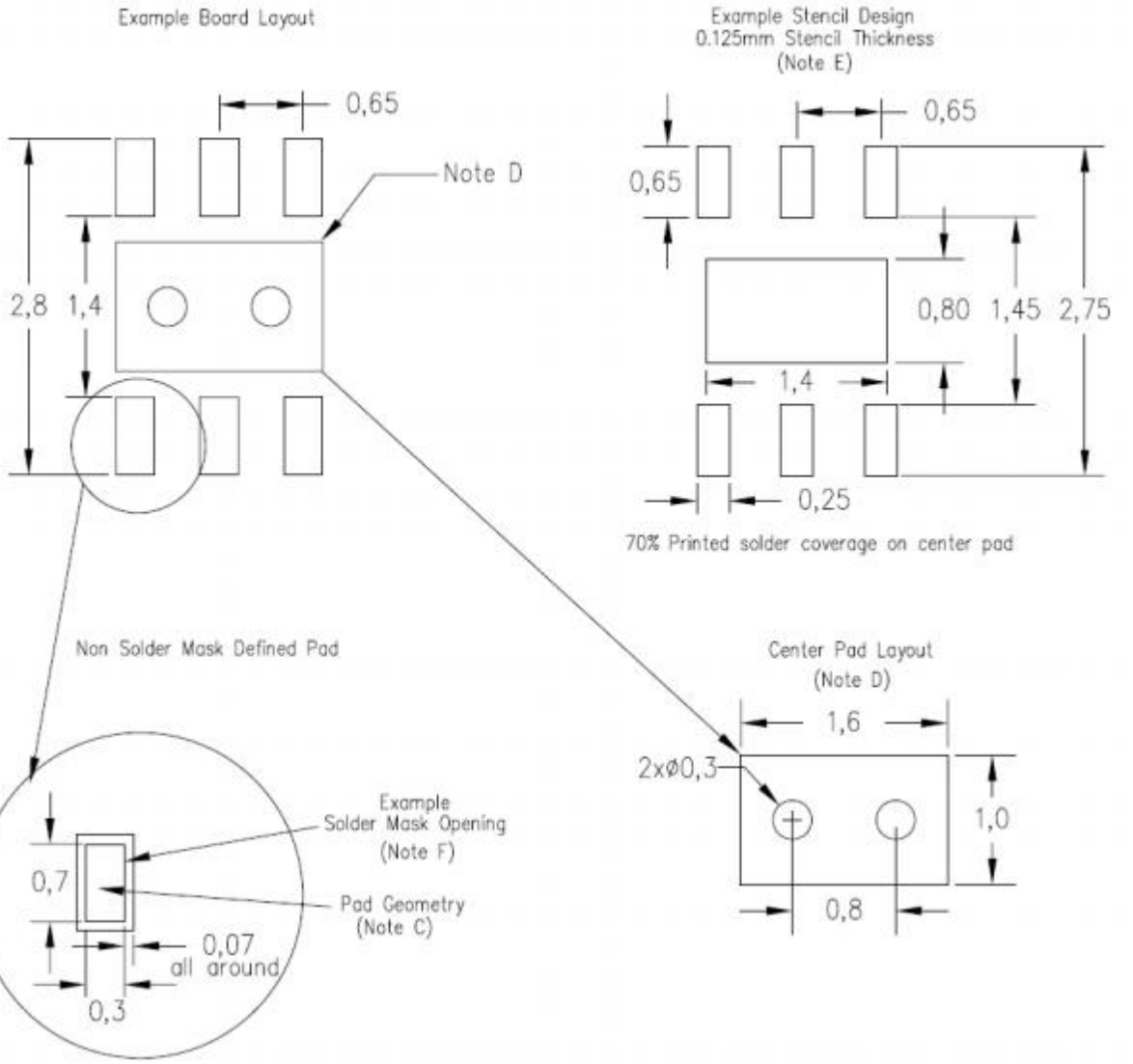
A3

COMMON DIMENSIIONS
(UNITS OF MEASURE=MILLIMETER

Symbol	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.20REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.90	1.00	1.10
E2	1.50	1.60	1.70
e	0.55	0.65	0.75
K	0.15	0.25	0.35
L	0.20	0.25	0.30
H		0.20REF	

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-229
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

LAND PATTERN DATA



NOTE A: All linear dimensions are in millimeters.

NOTE B: This drawing is subject to change without notice.

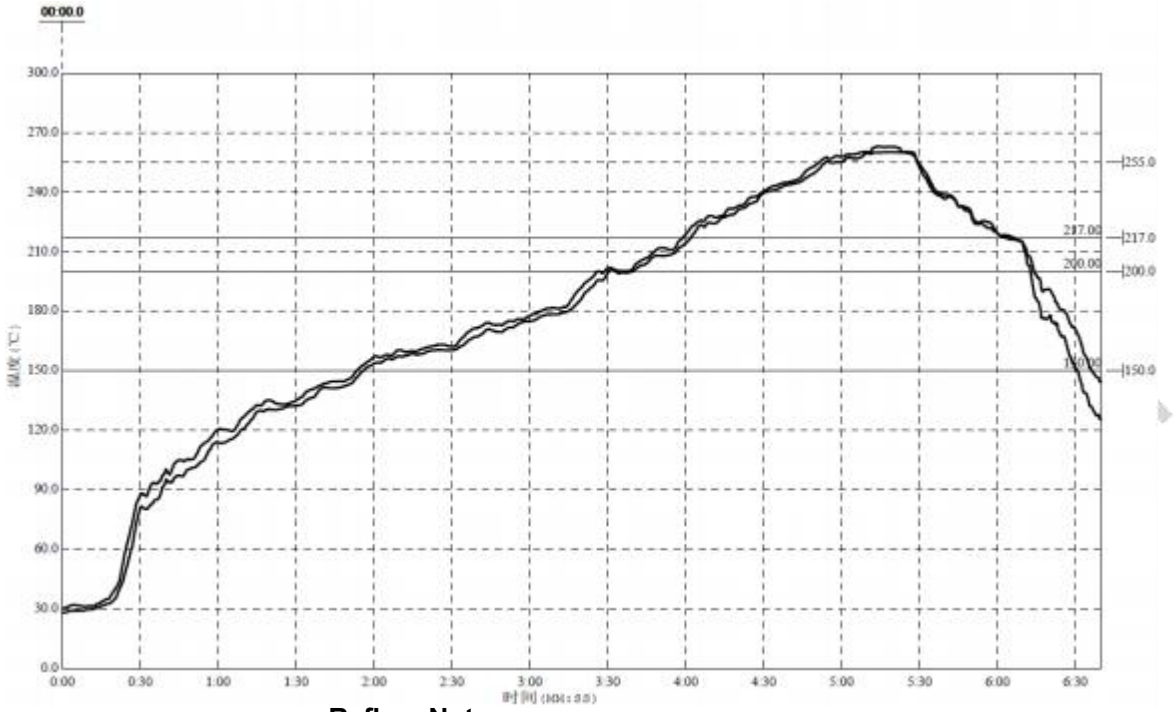
NOTE C: Publication IPC-7351 is recommended for alternate designs.

NOTE D: This land pattern is designed to be soldered to a thermal pad on the board.

NOTE E: Laser cutting aperture with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.

NOTE F: Customers should contact their board fabrication site for solder mask tolerances.

REFLOW



Reflow Note

Figure 24 Package Reflow Oven Thermal Profile

	Spec
Average ramp-up rate (217℃c to Peak)	Max. 3℃/sec
Time of Preheat temp.(from 150℃ to 200℃)	60-120sec
Time to be maintained above 217℃	60-150sec
Peak Temperature	>260℃
Time within 5℃ of actual peak temp	20-40sec.
Ramp-down rate	Max. 6℃/sec
Time from 25℃ to peak temp	Max. 8min.

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REVISION HISTORY

Vision	Date	Change Record
V0.9	June 2017	Datasheet V0.9 Released

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